GATE – SYLLABUS

Digital Electronics & Microprocessors

Transistor as a switching element; Boolean algebra, simplification of Boolean functions, Karnaugh Map and application; IC Logic gates and their characteristics; IC logic families: DTL, TTL, ECL, NMOS, PMOS and CMOS gates and their comparison; Combinational logic circuits; Half adder, full adder; Digital comparator; Multiplexer; ROM and their applications. Flip – flops, R – S, J – K, D and T flip – flops; Different types of counters and registers; waveform generators. A/D & D/A converters. Semiconductor memories. Microprocessor: Architecture, Programming, Memory and I/O Interfacing.
Digital Electronics & Microprocessors

INDEX

<table>
<thead>
<tr>
<th>Chapter No.</th>
<th>Contents</th>
<th>Page No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>01</td>
<td>Number Systems</td>
<td>1 – 12</td>
</tr>
<tr>
<td>02</td>
<td>Boolean Algebra &amp; Karnaugh Maps</td>
<td>13 – 20</td>
</tr>
<tr>
<td>03</td>
<td>Logic Gates</td>
<td>21 – 27</td>
</tr>
<tr>
<td>04</td>
<td>Logic Gate Families</td>
<td>28 – 35</td>
</tr>
<tr>
<td>05</td>
<td>Combinational Digital Circuits</td>
<td>36 – 41</td>
</tr>
<tr>
<td>06</td>
<td>Sequential Digital Circuits</td>
<td>42 – 46</td>
</tr>
<tr>
<td>07</td>
<td>Semiconductor Memories</td>
<td>47 – 50</td>
</tr>
<tr>
<td>08</td>
<td>A/D &amp; D/A Converters</td>
<td>61 – 53</td>
</tr>
<tr>
<td></td>
<td>Previous GATE Questions (Digital)</td>
<td>54 – 85</td>
</tr>
<tr>
<td>09</td>
<td>Introduction to Microprocessors</td>
<td>86 – 112</td>
</tr>
<tr>
<td></td>
<td>Previous GATE Questions (Microprocessors)</td>
<td>113 – 133</td>
</tr>
<tr>
<td>10</td>
<td>Public Sector Examination Questions</td>
<td>134 – 144</td>
</tr>
</tbody>
</table>

Profile

S. V. Rao, B.Sc., B.Tech., M.E.(Digital Systems), M.I.S.T.E., has been working for over 22 years, including the last 11 + years in the VLSI industry. Before joining the VLSI industry in 2000, he taught in the department of Electronics and Communication Engineering, JNTU Engineering College as an Associate Professor. He has also taught at the University College of Engineering, Osmania University and JNTU College of Engineering, Hyderabad and worked as a Lecturer at Dayan College of Engineering & Technology, Hyderabad.


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<table>
<thead>
<tr>
<th>S.NO</th>
<th>STUDENT NAME</th>
<th>GATE I.T NO</th>
<th>RANK</th>
</tr>
</thead>
<tbody>
<tr>
<td>01</td>
<td>SATISHKUMAR</td>
<td>CE 1639834</td>
<td>1</td>
</tr>
<tr>
<td>02</td>
<td>NETAJI PRASAD</td>
<td>CE6970996</td>
<td>2</td>
</tr>
<tr>
<td>03</td>
<td>ASHOK KUMAR</td>
<td>CE1430012</td>
<td>3</td>
</tr>
<tr>
<td>04</td>
<td>MOHD ATEF KAHAN</td>
<td>CE1459275</td>
<td>5</td>
</tr>
<tr>
<td>05</td>
<td>CHANDRAPAL RAM</td>
<td>CE2090202</td>
<td>10</td>
</tr>
</tbody>
</table>

#### MECHANICAL ENGINEERING TOPPERS

<table>
<thead>
<tr>
<th>S.NO</th>
<th>STUDENT NAME</th>
<th>GATE I.T NO</th>
<th>RANK</th>
</tr>
</thead>
<tbody>
<tr>
<td>01</td>
<td>DESAI HARDIKUMAR</td>
<td>ME1500097</td>
<td>7</td>
</tr>
<tr>
<td>02</td>
<td>KVVENKATACHALAPATHI</td>
<td>ME1500095</td>
<td>9</td>
</tr>
</tbody>
</table>

#### COMPUTER SCIENCE & ENGINEERING TOPPERS

<table>
<thead>
<tr>
<th>S.NO</th>
<th>STUDENT NAME</th>
<th>GATE I.T NO</th>
<th>RANK</th>
</tr>
</thead>
<tbody>
<tr>
<td>01</td>
<td>JITHIN VAHERY</td>
<td>CS758045</td>
<td>2</td>
</tr>
<tr>
<td>02</td>
<td>VENKATASAHYAKRISHNAD</td>
<td>CS1249099</td>
<td>10</td>
</tr>
</tbody>
</table>

#### ELECTRICAL ENGINEERING TOPPERS

<table>
<thead>
<tr>
<th>S.NO</th>
<th>STUDENT NAME</th>
<th>GATE I.T NO</th>
<th>RANK</th>
</tr>
</thead>
<tbody>
<tr>
<td>01</td>
<td>ANIL KUMAR A.</td>
<td>EE6240854</td>
<td>2 (Test series)</td>
</tr>
<tr>
<td>02</td>
<td>GHISH KUMAR DASARI</td>
<td>EE7650582</td>
<td>5 (Test series)</td>
</tr>
<tr>
<td>01</td>
<td>V. NARASIPPAUMURTHY</td>
<td>EE7646033</td>
<td>15</td>
</tr>
<tr>
<td>02</td>
<td>M. NAGARAJUreddy</td>
<td>EE7630195</td>
<td>14</td>
</tr>
<tr>
<td>03</td>
<td>THOKARI NITHENDU</td>
<td>EE1640320</td>
<td>18</td>
</tr>
</tbody>
</table>

#### ELECTRONICS & COMMUNICATION ENGINEERING TOPPERS

<table>
<thead>
<tr>
<th>S.NO</th>
<th>STUDENT NAME</th>
<th>GATE I.T NO</th>
<th>RANK</th>
</tr>
</thead>
<tbody>
<tr>
<td>01</td>
<td>M.YETHSWANTH</td>
<td>EE1440613</td>
<td>9</td>
</tr>
<tr>
<td>02</td>
<td>MOHD ATIF SHAHRAH WAIKIER</td>
<td>EE1444040</td>
<td>21</td>
</tr>
<tr>
<td>03</td>
<td>VENKATESHASASANAPURI</td>
<td>EE7490318</td>
<td>16</td>
</tr>
</tbody>
</table>

#### INSTRUMENTATION ENGINEERING TOPPERS

<table>
<thead>
<tr>
<th>S.NO</th>
<th>STUDENT NAME</th>
<th>GATE I.T NO</th>
<th>RANK</th>
</tr>
</thead>
<tbody>
<tr>
<td>01</td>
<td>MAHESH RAVI VARMA</td>
<td>IN1570517</td>
<td>1</td>
</tr>
<tr>
<td>02</td>
<td>MD ABDUL RAZAK</td>
<td>IN1570385</td>
<td>3</td>
</tr>
<tr>
<td>03</td>
<td>MAHESHWARI RUTHIKA</td>
<td>IN2300299</td>
<td>6</td>
</tr>
</tbody>
</table>

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### Chapter 1

#### Number Systems

The concept of counting is as old as the evolution of man on this earth. The number systems are used to quantify the magnitude of something. One way of quantifying the magnitude of something is by proportional values. This is called analog representation. The other way of representation of any quantity is numerical (Digital). There are many number systems are present. The most frequently used number systems in the applications of Digital Computers are Binary Number System, Octal Number System, Decimal Number System and Hexadecimal System.

The radix or Base (b) of a Number System: The Base or Radix of a number system is defined as the number of different symbols (Digits or Characters) used in that number system.

- The radix of Binary number system = 2 i.e. it uses two different symbols 0 and 1 to write the number sequence.
- The radix of Octal number system = 8 i.e. it uses eight different symbols 0,1,2,3,4,5,6,7 and 7 to write number sequence.
- The radix of Decimal number system = 10 i.e. it uses ten different symbols 0,1,2,3,4,5,6,7,8,9 to write number sequence.
- The radix of Hexadecimal number system = 16 i.e. it uses sixteen different symbols 0,1,2,3,4,5,6,7,8,9,A,B,C,D,E and F to write the number sequence.

To distinguish one number system from the other, the radix of the number system is used as a suffix to that number.

Eg: 10b Binary Number; 10o Octal Number; 10d Decimal Number; 16h Hexadecimal Number

Characteristics of any number system are:

1. Base or radix is equal to the number of digits in the system,
2. The largest value of digit is one (1) less than the radix, and
3. Each digit is multiplied by the base raised to the appropriate power depending upon the digit position.

The maximum value of digit in any number system is given by ($b-1$). Example: maximum value digit = in decimal number system $=$ ($10-1$) = 9.

Binary, Octal, Decimal and Hexadecimal number systems are called positional number systems.

The number system in which the weight of each digit depends on its relative position within the number, is called positional number system.

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Any positional number system can be expressed as sum of products of place value and the digit value.

Eg: \(756_{10} = 7 \times 10^2 + 5 \times 10^1 + 6 \times 10^0\)
\[156.24_{10} = 1 \times 10^2 + 5 \times 10^1 + 6.2 \times 10^0 + 4 \times 10^{-1}\]

The place values or weights of different digits in a mixed decimal number are as follows:
\[10^0 \times 10^1 \times 10^2 \times 10^3 \times 10^4 = \text{decimal point}\]

The place values or weights of different digits in a mixed binary number are as follows:
\[2^0 \times 2^1 \times 2^2 \times 2^3 = \text{binary point}\]

The place values or weights of different digits in a mixed octal number are as follows:
\[8^0 \times 8^1 \times 8^2 \times 8^3 = \text{octal point}\]

The place values or weights of different digits in a mixed octal number are as follows:
\[16^0 \times 16^1 \times 16^2 \times 16^3 = \text{Hexadecimal point}\]

**Decimal to binary conversion:**

(a) Integer number: Divide the given decimal number repeatedly by 2 and collect the remainders. This must continue until the integer quotient becomes zero.

\[
\begin{align*}
\text{Quotient} & \quad \text{Remainder} \\
37_{10} & \\
37/2 & = 18 + 0 \quad 0 \\
18/2 & = 9 + 0 \quad 0 \\
9/2 & = 4 + 1 \quad 1 \\
4/2 & = 2 + 0 \quad 0 \\
2/2 & = 1 + 0 \quad 0 \\
1/2 & = 0 + 1 \quad 1 \\
\end{align*}
\]
\[\therefore \boxed{37_{10} = 100101_2}\]

Note: The conversion from decimal integer to any base-\(r\) system is similar to the above example except that division is done by \(r\) instead of 2.

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(b) Fractional number: The conversion of a decimal fraction to a binary is as follows:
\[0.6875_{10} = X_2\]

First, 0.6875 is multiplied by 2 to give an integer and a fraction. The new fraction is multiplied by 2 to give a new integer and a new fraction. This process is continued until the fraction becomes 0 or until the number of digits has sufficient accuracy.

Integer value:
\[0.6875 	imes 2 = 1.3750\]
\[0.3750 	imes 2 = 0.7500\]
\[0.7500 	imes 2 = 1.5000\]
\[0.5000 	imes 2 = 1.0000\]
\[0.0000 = 0 \times (0.0875)\]

\[\therefore \boxed{0.6875_{10} = 0.1011_2}\]

**NOTE:** To convert a decimal fraction to a number expressed in base \(r\), a similar procedure is used. Multiplication is by \(r\) instead of 2, and the coefficients found from the integers may range in value from 0 to \((r-1)\).

The conversion of decimal number with both integer and fraction parts separately and then combining the results together.

Eg: \((41.6875)_{10} = X_8\)
\[41_{10} = 101001_2; 0.6875_{10} = 0.1011_2\]
\[\therefore \boxed{41.6875_{10} = 101001.1011_2}\]

Eg: Convert the Decimal number to its Octal equivalent: \(153_{10} = X_8\)

\[\begin{array}{c|c|c}
\text{Integer} & \text{Quotient} & \text{Remainder} \\
\hline
153 & 19 & \text{+1} \\
19 & 2 & \text{+3} \\
2/8 & = 0 & \text{+2} \\
\end{array}\]
\[\therefore \boxed{153_{10} = 231_8}\]

Eg: Convert \((0.513)_{10} = X_{16}\)
\[0.513 	imes 16 = 8.208 \\
0.208 	imes 16 = 3.328 \\
0.328 	imes 16 = 5.288 \\
0.288 	imes 16 = 4.608 \\
0.608 	imes 16 = 9.928 \\
0.928 	imes 16 = 14.848 \\
\[\boxed{0.513_{10} = 0.0.0048517..._{16}}\]

Eg: Convert \(253_{10}\) to hexadecimal
\[253/16 = 15 \text{ (13 = D)} \\
15/16 = 0 \text{ (15 = F)} \]
\[\therefore \boxed{253_{10} = 13\text{F}_{16}}\]

Eg: Convert the Binary number \(101101\); to decimal.
\[101101 = 2^5 + 2^4 + 2^3 + 2^2 + 2^1 + 2^0 = \boxed{85}\]

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\[ 32 + 8 + 4 + 1 = 45 \]
\[ (101011)_d = 45_{10} \]

Eg: Convert the Octal number 257 to decimal.
\[ 257_8 = 2 \times 8^2 + 5 \times 8^1 + 7 \times 8^0 = 128 + 40 + 7 = 175_{10} \]

Eg: Convert the Hexadecimal number 1AF23 to Decimal.
\[ 1AF23_{16} = 1 \times 16^4 + A \times 16^3 + F \times 16^2 + 2 \times 16^1 + 3 \times 16^0 = \]

**BCD (Binary Coded Decimal):** In this each digit of the decimal number is represented by its four bit binary equivalent. It is also called weighted BCD or 8421 code. It is a weighted code.

**Excess-3 Code:** This is an unweighted binary code used for decimal digits. Its code assignment is obtained from the corresponding value of BCD after the addition of 03.

**BCO (Binary Coded Octal):** In this each digit of the Octal number is represented by its three bit binary equivalent.

**BCH (Binary Coded Hexadecimal):** In this each digit of the hexadecimal number is represented by its four bit binary equivalent.

<table>
<thead>
<tr>
<th>Decimal Digits</th>
<th>BCD 8421</th>
<th>Excess-3</th>
<th>Octal digits</th>
<th>BCO Hexadecimal digits</th>
<th>BCH</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0000</td>
<td>0011</td>
<td>0</td>
<td>0</td>
<td>000</td>
</tr>
<tr>
<td>1</td>
<td>0011</td>
<td>0100</td>
<td>1</td>
<td>0</td>
<td>0005</td>
</tr>
<tr>
<td>2</td>
<td>0010</td>
<td>0101</td>
<td>2</td>
<td>0</td>
<td>0010</td>
</tr>
<tr>
<td>3</td>
<td>0011</td>
<td>0110</td>
<td>3</td>
<td>0</td>
<td>0011</td>
</tr>
<tr>
<td>4</td>
<td>0100</td>
<td>0111</td>
<td>4</td>
<td>0</td>
<td>0100</td>
</tr>
<tr>
<td>5</td>
<td>0101</td>
<td>1000</td>
<td>5</td>
<td>0</td>
<td>0101</td>
</tr>
<tr>
<td>6</td>
<td>0110</td>
<td>1001</td>
<td>6</td>
<td>0</td>
<td>0110</td>
</tr>
<tr>
<td>7</td>
<td>0111</td>
<td>1010</td>
<td>7</td>
<td>0</td>
<td>0111</td>
</tr>
<tr>
<td>8</td>
<td>1000</td>
<td>1011</td>
<td>8</td>
<td>R</td>
<td>1000</td>
</tr>
<tr>
<td>9</td>
<td>1001</td>
<td>1100</td>
<td>9</td>
<td>A</td>
<td>1010</td>
</tr>
<tr>
<td>10</td>
<td>1010</td>
<td></td>
<td>10</td>
<td>B</td>
<td>1011</td>
</tr>
<tr>
<td>11</td>
<td>1011</td>
<td></td>
<td>11</td>
<td>C</td>
<td>1100</td>
</tr>
<tr>
<td>12</td>
<td>1100</td>
<td></td>
<td>12</td>
<td>D</td>
<td>1101</td>
</tr>
<tr>
<td>13</td>
<td>1101</td>
<td></td>
<td>13</td>
<td>E</td>
<td>1110</td>
</tr>
<tr>
<td>14</td>
<td>1110</td>
<td></td>
<td>14</td>
<td>F</td>
<td>1111</td>
</tr>
</tbody>
</table>

Don't care values or unused states in BCD code are 1010, 1011, 1100, 1101, 1110, 1111.

Don't care values or unused states in excess-3 code are 0000, 0001, 0100, 1001, 1100, 1111.

The binary equivalent of a given decimal number is not equivalent to its BCD value.
Eg: 254 \(_{10} = 11001_2 \)

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The BCD equivalent of decimal number 25 \(_{10} = 00101001\) from the above example the BCD value of a given decimal number is not equivalent to its straight binary value.

The BCO (Binary Coded Octal) value of a given Octal number is exactly equal to its straight binary value.
Eg: 25\(_4 = 21\(_8 = 10101_2 \)

The BCO value of 25\(_4 = 031_8 \)
From the above example, the BCO value of a given Octal number is same as its binary equivalent of the same number.

The BCH (Binary Coded Hexadecimal) value of a given hexadecimal number is exactly equal to its straight binary.
Eg: 25\(_{16} = 37\(_8 = 1010101_2 \)

The BCH value of hexadecimal number 25\(_{16} = 00100101_2 \)
From this example the above statement is true.

<table>
<thead>
<tr>
<th>(0/1)'s Complement</th>
<th>r's Complement</th>
<th>Binary</th>
<th>Octal</th>
<th>Decimal</th>
<th>Hexadecimal</th>
</tr>
</thead>
<tbody>
<tr>
<td>1's</td>
<td>2's</td>
<td>r2's</td>
<td>2's</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>2's</td>
<td>1's</td>
<td>r2's</td>
<td>2's</td>
<td>10</td>
<td>10</td>
</tr>
</tbody>
</table>

Rules of Binary addition: 0 + 0 = 0; 0 + 1 = 1; 1 + 0 = 1; 1 + 1 = 0
Carry

Rules of Binary subtraction: 0 - 0 = 0; 0 - 1 = 1; 1 - 1 = 0; 1 - 0 = 1
Barrow

Example: Add the two binary numbers 101101.
Addend 101101

Sum 1010100

Example: Subtract the binary number 100111 from 101101.
Minuend 101101
Subtrahend 100111

Difference 000100

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Example: Multiply the Binary number 1011, with 1011.

Multiplier: X 1011

1011
0000
1011

Product: 110011

Example: 11011 + 11
110111
11
11
Quotient = 110
Remainder = 1.

While storing the signed binary numbers in the internal registers of a digital computer, most significant bit position is always reserved for sign bit and the remaining bits are used for magnitude.

\[
\begin{array}{c|c|c|c|c|c|c|c|c|c}
\text{Sign} & A_7 & A_6 & A_5 & A_4 & A_3 & A_2 & A_1 & A_0 \\
\hline
\end{array}
\]

Fixed Point Representation and Floating Point Representation:

The representation of the decimal point (or binary point) is always fixed in one position. The two positions most widely used are (1) a decimal point in the extreme right of the register to make the stored number a fraction, and (2) a decimal point in the position of the decimal point in a register.

\[
\begin{align*}
\text{Fixed point fraction} & \quad \text{Fixed point integer} \\
\end{align*}
\]

The floating-point representation uses a second register to store a number that designates the position of the decimal point in the first register.

Positive numbers are stored in the register of digital computer in sign-magnitude form only.

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Negative numbers can be represented in one of three possible ways.
1. Signed-magnitude representation.
2. Signed-1’s complement representation.

Example: +9

<table>
<thead>
<tr>
<th>Sign</th>
<th>Magnitude</th>
<th>+9 0001001</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0 0001</td>
<td>+9 0001001</td>
</tr>
<tr>
<td></td>
<td>1 1110</td>
<td>-9 1110100</td>
</tr>
<tr>
<td></td>
<td>1 1110</td>
<td>-9 1110100</td>
</tr>
</tbody>
</table>

The 2’s complement of a given binary number can be formed by leaving all least significant zeros and the first non-zero digit unchanged, and then replacing 1’s by 0’s and 0’s by 1’s in all other higher significant digits.

Example: The 2’s complement of 10011000, is 11010100.

Subtraction using 2’s complement: Represent the negative numbers in signed 2’s complement form, add the two numbers, including their sign bit, and discard any carry out of the most significant bit.

Since negative numbers are represented in 2’s complement form, negative results also obtained in signed 2’s complement form.

Example: 1’s complement:

| +6 0000110 | +6 0001100 |
| +9 0001001 | -9 1110100 |
| +15 0001111 | -15 1101111 |

| Carry +1 |
| 0 0000111 |

Example: 2’s complement:

| -6 111010 | +6 000110 |
| +9 0001001 | -9 1110100 |
| +15 0001111 | -15 1101111 |

Note: The advantage of signed 2’s complement representation over the signed-1’s complement form (and the signed-magnitude form) is that it contains only one type of zero.

The range of binary integer numbers that can be accommodated in a register of length n-bits using signed-1’s complement form is given by \((-2^{n-1})\) to \((-2^{n-1}-1\) which includes both types of zero i.e., 0 and -0. For example if n = 8, then range is +127 to -127.

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The range of integer binary numbers that can be accommodated in a register of $n$-bit length by using signed 2's complement representation is given by $-2^{n-1} \leq x \leq 2^{n-1} - 1$ which includes only one type of zero i.e., $+0$.

For example if $n = 8$, then range is $+127$ to $-128$.

2's complement form is usually chosen over 1's complement to avoid the occurrence of a negative zero. 2's complement of zero is zero only.

The 1’s complement of 1’s complement of a given number is the same number itself.

The general form of floating-point number is $m \times e$. Where $M = Mantissa$, $r = base$, $e = exponent$. Example: $0.3574 \times 10^3$.

The Mantissa can be a fixed point fraction or fixed point integer.

Normalization: Getting non-zero digit in the most significant digit position of the mantissa is called Normalization.

if the floating point number is normalized, more number of significant digits can be stored, as a result accuracy can be improved.

A zero cannot be normalized because it does not contain a non-zero digit.

The hexadecimal code is widely used in digital systems because it is very convenient to enter binary data in a digital system using hexadecimal code.

The parity of a digital word is used for detecting error in digital transmission.

In weighted codes, each position of the number has specific weight. The decimal value of a weighted code number is the algebraic sum of the weights of those positions in which 1’s appear.

Most frequently used weighted codes are 8421, 2421 code, 5211 code and 84 271 code.

Example: The decimal number 403 is represented in different codes as

- In 8421 code: 0110 0100 0111
- In 2421 code: 0100 1111 0011
- In 5211 code: 0011 1111 0101
- In 84 271 code: 0100 1111 0101

Reflective Code: A code is called effective or self-complementing if the code for 9 is the complement of the code for 0, code for 8 is the complement from 1 and so on. 2421, 84271, 5211 are examples for reflected codes.

Sequential Code: A code is called sequential if each successive code is one binary number greater than its preceding code. Example: 8421

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1. The number system with radix 2 is known as (a) Binary (b) Decimal (c) Octal (d) Hexadecimal

2. A group of four bits is known as (a) Bit (b) Byte (c) Oddle (d) Word

3. The knowledge of binary number system is required for the designers of computer and other digital systems because (a) It is easy to learn binary number system (b) It is easy to learn Boolean algebra (c) It is easy to use binary codes (d) The devices used in these systems operates in binary

4. The ones complement of the binary number 10001011 is (a) 01110100 (b) 11111111 (c) 01110101 (d) 11111110

5. The twos complement of the number 10010100 is (a) 01101010 (b) 10101011 (c) 01101001 (d) None

6. The ones complement of the given binary number is (a) Some binary number (b) Zero (c) Non-numeric (d) None

7. The twos complement of the ones complement of the given binary number 101101 is (a) 101000 (b) 100011 (c) 101001 (d) 010011

8. The base or radix of hexadecimal number system is (a) 2 (b) 8 (c) 16 (d) 15

9. The number system with base or radix 8 is known as (a) Binary (b) Decimal (c) Octal (d) Hexadecimal

10. The decimal equivalent of the binary number 101101 is (a) 48 (b) 45 (c) 57 (d) 75

11. The decimal equivalent of the binary number 1001.0101 is (a) 9.125 (b) 9.625 (c) 9.375 (d) 9.625

12. The binary equivalent of decimal number 255 is (a) 11111110 (b) 11111111 (c) 11111111 (d) None

13. Identify the binary number represented by the decimal number 10.625 (a) 1010.1N1 (b) 1010.101 (c) 1010.1010 (d) None

14. The binary equivalent of the decimal number 0.625 is (a) 0.1010 (b) 0.1011 (c) 0.1101 (d) 0.0110

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Number Systems

15. The octal equivalent of the decimal number 375 is (a) 560 (b) 567 (c) 563 (d) None

16. The octal equivalent of the decimal number 27.125 is (a) 33.23 (b) 33.38 (c) 33.1 (d) 33.01

17. The decimal equivalent of the octal number 237 is (a) 159 (b) 165 (c) 162 (d) 160

18. The hexadecimal equivalent of the decimal number 32 is (a) 17 (b) 1A (c) 1F (d) None

19. The decimal equivalent of the hexadecimal number “DDEE” is (a) 47877 (b) 48877 (c) 46777 (d) None

20. Encode the decimal number 327 187 in BCD code (a) 0010001 011101 100001 100011 00101111 11001010 (b) 0010 0010 1111 0101 1010 1000 0111 1010 1000 0111 (c) 11011 0010 0101 1001 0001 0010 1011 0011 1010 1000 0111 (d) None

21. The decimal equivalent of the hexadecimal number 3A.7F is (a) 58.1835 (b) 58.1385 (c) 58.23 (d) None

22. The decimal number 13 is represented in natural BCD as (a) 1101 (b) 0001 0011 (c) 0000 1101 (d) None

23. The binary equivalent of the hexadecimal number A8B is (a) 1010 1000 1011 0101 (b) 1010 1000 1010 0101 (c) 1010 1000 1011 0101 (d) None

24. The octal equivalent of the binary number 1101111 is (a) 656 (b) 32 (c) 653 (d) D7

25. The decimal equivalent of the binary number 1010111 is (a) 215 (b) 225 (c) 250 (d) None

26. The octal equivalent of the decimal number 215 is (a) 237 (b) 372 (c) 237 (d) None

27. The maximum positive and negative numbers which can be represented in two-complement form using n bits are respectively (a) 2^n-1, -2^n+1 (b) 2^n+2, -2^n (c) 2^n-1, -2^n (d) 2^n-1, -2^n+1

28. When two n-bit binary numbers are added then the sum contains at most (a) 0 bits (b) (n+1) bits (c) (n+2) bits (d) (n+1) bits

29. The largest positive number that can be stored in a computer that has 16-bit word length and uses two complement arithmetic is (a) 32 (b) 32767 (c) 32768 (d) 65536
Chapter 2: Boolean algebra & Karnaugh Maps

POINTS TO REMEMBER

- Boolean algebra works with binary variables.
- A Boolean algebra is an algebraic system consisting of the set {0,1}, the binary operations called OR, AND, or NOT denoted by the symbols "+", "", and "prime".
- Boolean algebra enables the logic designer to simplify the circuit used, achieving economy of construction and reliability of operation.
- Boolean algebra suggests the economic and straightforward way of describing the circuitry used in any computer system.
- Boolean algebra is unique in the way that it takes only two different values either 0 or 1. It does not have negative number. It does not have fraction number.
- The basic Boolean postulates:

  Logical Multiplications based on AND function.
  1. 0 . 0 = 0
  2. 0 . 1 = 0
  3. 1 . 0 = 0
  4. 1 . 1 = 1

  Logical Additions based on OR function
  1. 0 + 0 = 0
  2. 0 + 1 = 1
  3. 1 + 0 = 1
  4. 1 + 1 = 1

  Complement based on NOT function.
  9. 0' = 1
  10. 1' = 0

- Boolean properties:
  a) Properties of AND function
  1. X.0 = 0
  2. X.1 = X
  3. X.1 = X
  4. 1.X = X
b) Properties of OR function
5. \( X + 0 = X \)
6. \( 0 + X = X \)
7. \( X + 1 = 1 \)
8. \( 1 + X = 1 \)

c) Combining a variable with itself or its complement
9. \( X \cdot X = 0 \)
10. \( X \cdot \overline{X} = X \)
11. \( X \cdot \overline{X} = \overline{X} \cdot X = X \)
12. \( X \cdot \overline{X} = 1 \)
13. \( \overline{X} \cdot \overline{Y} = \overline{X} \cdot \overline{Y} \)

d) Commutative laws:
14. \( x \cdot y = y \cdot x \)
15. \( x + y = y + x \)

e) Distributive laws:
16. \( x(y + z) = xy + xz \)
17. \( x + yz = (x + y)(x + z) \)

f) Associative laws:
18. \( x(yz) = (xy)z \)
19. \( x + (y + z) = (x + y) + z \)

g) Absorption laws:
20. \( x \cdot x + y = x \)
21. \( x \cdot \overline{x} + y = x \)
22. \( x + x \cdot y = x + y \)
23. \( x + \overline{y} = x \cdot \overline{y} \)

h) De Morgan’s laws.
24. \( (x + y)' = x' \cdot y' \)
25. \( (x \cdot y)' = x' + y' \)

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Boolean Algebra & Karnaugh Maps

> In Boolean algebra, ‘1’ is called multiplicative identity and ‘0’ is called additive identity.

> Literal: A primed or unprimed Boolean variable is called literal. Each variable can have a maximum of two literals. Example: \( x \) is a variable which can have two literals \( x \) and \( x' \).

Proof for some important properties:

17. \( xy + yz = (xy)(xy + yz) \)
\( = xz + xy + yz \)
\( = x(z + yz) \)
\( = x + yz \)

since \( 1 + 0 = 1 \)

22. \( x + x'y = x'y \)
\( = x + xy + y = x + y \)

since \( 1 + 0 = 1 \)

Logic Circuits can be simplified by pairing the Boolean equations using any one of the following methods:

a) Applying Boolean properties
b) Karnaugh-map method of simplification
c) Tabulation method.

Boolean properties can be applied successively to minimize the given Boolean equation. But there is no guarantee that always we get minimal equation in this method.

2, 3 and 4 variable equations can be simplified to minimal value quickly using K-map method.

Tabulation method is used to minimize the equations with high order variables.

The properties of Boolean Algebra are useful for the simplification of Boolean equation leading to minimal gate structure.

Simplify the Boolean equation \( x + xy = x + y \).
\( = (x + x'y) + y \)
\( = (x + y') + y \)

---

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Duality Principle: The important property of Boolean algebra is the duality principle. It states that every algebraic expression deductible from theorems of Boolean algebra remains valid if the operators and identify elements are interchanged.

Examples:

\( x \cdot x = x \) 
\( x + 1 = 1 \) 
\( x + y = x \) 
\( x \cdot y = y \cdot x \) 
\( x + (y + z) = (x + y) + z \) 

The dual of the exclusive-OR is equal to its complement.

A simple procedure to find the complement of a function is to take the dual of the function and complement each literal.

Standard Product or a minterm (m): Consider two binary variables \( x \) and \( y \) combined with an \( \text{AND} \) operation. Since each variable appears in direct form or in its complement form there are two possible combinations: \( X \cdot Y, X \cdot Y \), \( X \cdot Y \), and \( X \cdot Y \). Each of these four \( \text{AND} \) terms is called a minterm or a standard product term.

<table>
<thead>
<tr>
<th>( X )</th>
<th>( Y )</th>
<th>( \text{minterm (m)} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>( X \cdot Y )</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>( X \cdot Y )</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>( X \cdot Y )</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>( X \cdot Y )</td>
</tr>
</tbody>
</table>

Standard sum or Maxterm (M): Two binary variables \( x \) and \( y \) combined with an \( \text{OR} \) operation we will get four possible combinations \( X + Y, X + Y, X + Y \), and \( X + Y \). Each of these four \( \text{OR} \) terms is called a maxterm or a standard sum term.

<table>
<thead>
<tr>
<th>( X )</th>
<th>( Y )</th>
<th>( \text{Maxterms (M)} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>( X + Y )</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>( X + Y )</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>( X + Y )</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>( X + Y )</td>
</tr>
</tbody>
</table>

Maxterm is the compliment of its corresponding Minterm and vice versa.

Eg: \( X \cdot Y \) = minterm.

The compliment of minterm = \( (X \cdot Y) \) = \( X + Y \) = maxterm

Boolean Algebra & Karnaugh Maps

Canonical form: Expressing the Boolean function in Standard Sum of Product form (SSOP) or Standard Product of Sums form (SPOS) is called Canonical form.

A Boolean function may be expressed algebraically from a given truth table by forming a minterm for each combination of the variables which produces a 1 in the function, and then taking the OR of all those terms.

<table>
<thead>
<tr>
<th>( X )</th>
<th>( Y )</th>
<th>( F )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

\( F(X, Y) = X \cdot Y + X \cdot Y = \Sigma m(1, 2) \). This representation is called SSOP form.

A Boolean function may be expressed algebraically from a given truth table by forming the maxterms for each combination of the variables which produces zero '0' in the function, and then taking the AND of all those terms.

<table>
<thead>
<tr>
<th>( X )</th>
<th>( Y )</th>
<th>( F )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

\( F = (X + Y)(X' + Y') = \Pi M(3) \). This representation is called SPOS form.

If one canonical form is given it is possible to express other canonical form.

Example: The other canonical form of the equation \( F(X, Y, Z) = \Pi M(0, 2, 3, 6) \) is

\( F(X, Y, Z) = \Sigma m(1, 4, 5, 7) \).

Sum of all the minterms of \( x \) given Boolean function is equal to 1.

Example: \( F(X, Y, Z) = \Sigma m(0, 1, 2, 3, 4, 5, 6, 7) = 1 \)
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> Product of all the maxterms of a given Boolean function is equal to 0.

Example: \( F(X,Y,Z) = \overline{1}M(0,1,2,3,4,5,6,7) = 0. \)

> Boolean functions expressed as a sum of minterms or product of maxterms are said to be in canonical form.

> Sum of products form can be implemented by using two-level gate network NAND-NAND logic.

> NAND-NAND realization is same as AND-OR.

> Product of sums form can be implemented by using two-level gate network NOR-NOR logic.

> NOR-NOR realization is same as OR-AND.

> If the signals are propagating through two stages of gates, then it is called two-level gate network.

> Degenerative Form: A two-level gate network is said to be degenerative if it degenerates to a single operation.

   Example: AND - AND is equivalent to AND

> The following two-level gate networks are Degenerative forms:

   \[
   \begin{array}{cccc}
   \text{AND} & \text{AND} & \text{AND} \\
   \text{OR} & \text{OR} & \text{OR} \\
   \text{OR} & \text{NOR} & \text{NOR} \\
   \text{AND} & \text{NAND} & \text{NAND} \\
   \text{NOR} & \text{NAND} & \text{OR} \\
   \text{NAND} & \text{NOR} & \text{AND} \\
   \end{array}
   \]

   KARNAUGH MAPS (K-maps):

   > A map is a diagram made up of squares. Each square represents either a minterm or a maxterm.

   > The number of squares in the Karnaugh map is given by \( 2^n \) where \( n \) = number of variable.

   > Two variable K-map consists of 4-cells or squares.

   > Three variable K-map consists of 8-squares or 8 cells.

   > Four variable K-map consists of 16-squares or 16 cells.

   > To maintain adjacency property Gray code sequence is used in K-maps. (Any two adjacent cells will differ by only one bit).

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Boolean Algebra & Karnaugh Maps

> Two variable K-map:

Each cell represents a term of two literals.

Grouping two adjacent (pair) squares containing 1's represents a term of one literal.

Grouping four adjacent squares containing 1's represent the function = 1.

<table>
<thead>
<tr>
<th>( x )</th>
<th>( y )</th>
<th>( xy )</th>
<th>( xy )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

> Three variable K-map:

Each cell represents a term of three literals.

Grouping two adjacent cells containing 1's (Pair) represent a term of two literals.

Grouping four adjacent cells containing 1's (Quad) represents a term of one literal.

Grouping eight adjacent cells containing 1's represents the function = 1.

> Four variable K-map:

Each cell or square represents one minterm, giving a term of four literals.

Grouping two adjacent squares containing 1's represents a term of three literals.

Grouping four adjacent squares containing 1's represents a term of two literals.

Grouping eight adjacent squares containing 1's represents a term of one literal.

Grouping sixteen adjacent squares containing 1's represent the function = 1 (a term of zero literals).

Rules to simplify K-maps: 1. At the time of grouping the adjacent cells containing 1's always use maximum possible group. 2. All the cells containing 1's must be covered at least once in any group. 3. At the time of grouping don't care (X) values can be taken as 1's. 4. All don't care values need not be covered.

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Chapter 3

LOGIC GATES

POINTS TO REMEMBER

- A gate is an electronic circuit with one output and one or more inputs. The output always depends on the input combinations.

- AND, OR and NOT gates are called Basic gates.

- NAND and NOR gates are called Universal gates, because, by using only NAND gates or by using only NOR gates we can realize any gate or any circuit.

- Special gates are Exclusive-OR gate and Exclusive-NOR gate.

- Exclusive-NOR (X-NOR) gate is also called inclusive-OR or gate of equivalence.

- There are two types of logic systems:

  (a) Positive level logic system

  (b) Negative level logic system

- Positive level logic system (PLLS): Out of the given two voltage levels, the more positive value is assumed as logic ‘1’ and the other as logic ‘0’.

<table>
<thead>
<tr>
<th>Logic ‘0’</th>
<th>Logic ‘1’</th>
</tr>
</thead>
<tbody>
<tr>
<td>0V</td>
<td>5V</td>
</tr>
<tr>
<td>-2V</td>
<td>+7V</td>
</tr>
<tr>
<td>-7V</td>
<td>-2V</td>
</tr>
<tr>
<td>+2V</td>
<td>+7V</td>
</tr>
</tbody>
</table>

Example 1:

- Negative level logic system (NLLS): Out of the given two voltage levels, the more negative value is assumed as logic ‘1’ and the other as logic ‘0’.

<table>
<thead>
<tr>
<th>Logic ‘1’</th>
<th>Logic ‘0’</th>
</tr>
</thead>
<tbody>
<tr>
<td>0V</td>
<td>5V</td>
</tr>
<tr>
<td>-2V</td>
<td>+7V</td>
</tr>
<tr>
<td>+7V</td>
<td>-2V</td>
</tr>
<tr>
<td>+2V</td>
<td>+7V</td>
</tr>
</tbody>
</table>

Example:
\( \rightarrow \text{AND gate:} \) "The output of AND gate is high if all the inputs are high." (or) "The output of AND gate is low if any one input is low or all the inputs are low."

<table>
<thead>
<tr>
<th>( A )</th>
<th>( B )</th>
<th>( Y )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Internal Circuit diagram of AND gate with positive level logic system.

\( \rightarrow \text{OR gate:} \) "The output of an OR gate is high if any one input is high or all inputs are high." (or) "The output of an OR gate is zero if all the inputs are zeros."

<table>
<thead>
<tr>
<th>( A )</th>
<th>( B )</th>
<th>( Y )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Internal Circuit diagram of OR gate with positive level logic system.

\( \rightarrow \) The circuit, which is working as AND gate with positive level logic system, will work as OR gate with negative level logic system.

\( \rightarrow \) The circuit, which is working as OR gate with positive level logic system, will work as AND gate with negative level logic system.

\( \rightarrow \) Truth table is also called table of combinations.

\( \rightarrow \) The number of rows in the truth table is given by \( 2^n \) where 'n' is the number of inputs to the gate.

\( \rightarrow \text{NOT gate:} \) It is also called inverter. "The output of a NOT gate is always compliment of the input".

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\[ Y = A \oplus B = AB' + A'B \]

**Realization of Basic gates using NAND and NOR gates:**

1. **NOR gate**
   - \[ Y = \overline{A} \]
   - \[ Y = (A \cdot A)' = (A + A)' = A' \]

2. **AND gate**
   - \[ Y = AB \]
   - \[ Y = AB' + A'B \]

**OR Gate**

\[ Y = A + B \]

**Realization of NAND gate using NOR gates:**

\[ Y = (A \cdot B)' \]

**Realization of NOR gate using NAND gates:**

\[ Y = (A + B)' \]

**Realization of X-OR gate using NAND and NOR gates:**

\[ Y = AB' + A'B \]

The minimum number of NAND gates required to realize X-OR gate is four.

The minimum number of NOR gates required to realize X-OR gate is five.
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Realization of X-NOR gate using NAND and NOR gates:

\[ Y = \overline{A \cdot B} + \overline{A} \cdot B \]

\[ Y = \overline{A} \cdot B + A \cdot \overline{B} \]

The minimum number of NAND gates required to realize X-NOR gate is 5.
The minimum number of NOR gates required to realize X-NOR gate is 4.

Alternate logic gate symbols: The alternate logic gate symbols for the standard gate symbols are obtained by interchanging AND and OR symbols, and by interverting all inputs and outputs.

A bubbled NAND gate is equivalent to OR gate:

\[ Y = (A \cdot B)' = A + B \]

A bubbled NOR gate is equivalent to AND gate:

\[ Y = A \cdot B \]

A bubbled AND gate is equivalent to NOR gate:

\[ Y = (A \cdot B)' = A + B \]

A bubbled OR gate is equivalent to NAND gate:

The alternate logic gate symbols for the standard gates are obtained based on De Morgan's laws only.

Equivalence Properties:
1. \((X \oplus Y) = X \cdot Y + X \cdot Y\)
2. \(X \cdot Y = \overline{X} \cdot \overline{Y}\)
3. \(X \cdot Y = X \)
4. \(X \cdot X = 1\)
5. \(X \cdot Y = 0\)
6. \(Y \cdot Y = X \cdot Y\)
7. \(X \cdot Y = X \cdot Y\)

Notes:

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Logic Gates

A bubbled OR gate is equivalent to NAND gate.

\[ Y = (A \cdot B)' \]

The alternate logic gate symbols for the standard gates are obtained based on De Morgan's laws only.

Equivalence Properties:
1. \((X \oplus Y) = X \cdot Y + X \cdot Y\)
2. \(X \cdot Y = \overline{X} \cdot \overline{Y}\)
3. \(X \cdot Y = X \)
4. \(X \cdot X = 1\)
5. \(X \cdot Y = 0\)
6. \(Y \cdot Y = X \cdot Y\)
7. \(X \cdot Y = X \cdot Y\)

Notes:

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Chapter - 4  LOGIC GATE FAMILIES

POINTS TO REMEMBER
- Digital IC gates are classified not only by their logic operation, but also by the specific logic circuit family to which they belong. Each logic family has its own basic electronic circuit upon which more complex digital circuits and functions are developed.
- Different types of logic gate families:
  - RTL: Resistor-transistor logic gate family.
  - DCTL: Direct-coupled Transistor Logic gate family.
  - RCTL: Resistor-capacitor-transistor logic.
  - DTL: Emitter Transistor Logic gate family.
  - TTL: Transistor Logic gate family.
  - IL: Integrated Injection Logic.
  - HTL: High Threshold Logic.
  - ECL: Emitter-coupled logic.
  - MOS: Metal Oxide Semi-conductor.
  - CMOS: Complementary Metal Oxide Semi-conductor.
- HTL is a modified form of DTL and IL is a modified form of DCTL.
- Because of high package density MOS and PL logic gate families are used for Large Scale integration (LSI) functions.
- TTL, ECL, and CMOS are used for Medium Scale Integration (MSI) or Small Scale Integration (SSI).
- Each logic gate family is identified with a series number. For example, TTL family ICs are available in 74/54 series. Each logic family is numbered appropriately. TTL and CMOS ICs have 4000 series and ECL family has 10000 series.
- RTL, DTL, ECL and PL Logic families use bipolar transistors. Hence these families are called bipolar logic gate families.
- MOS and CMOS families use unipolar transistors called Metal-Oxide-Semiconductor Field-effect Transistors (MOSFETS). Hence these families are called unipolar logic gate families.

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- Fan-out: "The number of standard loads that the output of the gate can drive without distorting its normal operation".
- Fan-in: "The maximum number of inputs that can be applied to the logic gate".
- Power dissipation: "The power consumed per gate".
- Propagation Delay: "The average transition delay time for the signal to propagate from input to output when the signal changes value".
- Noise Margin: "It is the limit of a noise voltage which may be present without impairing the proper operation of the circuit".
- Figure of Merit: The product of propagation delay time and power dissipation is known as figure of merit of performance of a gate. Normally minimum value is desired.
- Logic Swing: The difference between the two output voltages (VDD-VOL) is known as the logic swing of the circuit.
- Noise Immunity: "The ability of the circuit to withstand variations in the input levels".
- Saturation logic: A form of logic gates in which one output state is the saturation voltage level of the transistor. Example: RTL, DTL, TTL.
- Unsaturation logic or Current Mode Logic: A form of logic with transistors operated outside the saturation region. Example: CML or ECL.
- ECL has ultra-fast switching speed and low logic swing.
- The temperature range of 74-series of TTL logic gate family is 0°C to 70°C. This series of ICs is used for commercial applications.
- The temperature range of 34-series of TTL logic gate family is −55°C to 125°C. This series of ICs is used for Military applications.
- Voltage parameters of the digital IC:
  - High-level input voltage, VIL: This is the minimum input voltage which is recognized by the gate as logic 1.
  - Low-level input voltage, VIH: This is the maximum input voltage which is recognized by the gate as logic 0.
  - High-level output voltage, VOH: This is the minimum voltage available at the output corresponding to logic 1.
  - Low-level output voltage, VOL: This is the maximum voltage available at the output corresponding to the logic 0.

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- The number of various functions available in a logic family is known as the breadth of the logic family.
- When the outputs of logic gates are connected together additional logic functions are performed. This is known as wired-logic.
- When the outputs are available in complemented as well as uncomplemented form it is referred to as complementary outputs. This eliminates the need of using additional inverters.
- Passive pull-up: In a bipolar logic circuit, a resistor R<sub>c</sub> used in the collector circuit of the output transistor is known as passive pull-up.
- Active pull-up: In a bipolar logic circuit a 0JT and diode circuit used in the collector circuit of the output transistor instead of R<sub>c</sub> is known as active pull-up. This facility is available in TTL family.
- The advantages of active pull-up over passive pull up are increased speed of operation and reduced power dissipation.
- Open collector output: In a bipolar logic circuit if nothing is connected at the collector of the output transistor and this collector terminal is available as IC pin, it is known as open-collector output.
- Tri-state logic: In the tri-state logic, in addition to low impedance 0 and 1 there is a third state known as the high-impedance state. When the gate is disabled it is in the third state.
- In TTL logic gate family there different types of output configurations are available: they are Open-collector output type, Emitter-pole output type and tri-state output type.
- The advantages of open-collector output type are wired-logic can be performed and loads other than the normal gate can be used.
- The tri-state logic devices are used in bus oriented systems.
- If any input of TTL circuit is left floating, it will function as if it is connected to logic 1 level.
- The supply voltage range of 74-series is 5 ± 0.25V and for 54-series is 5 ± 0.5V.
- Negative supply is preferred in ECL family because, the effect of noise present in the supply line is reduced considerably and any accidental short-circuiting of output to ground will not damage the gate.
- MOS logic is widely used in LSI and VLSI applications because the silicon chip area required for fabrication of a MOS device is very small.
- The fan-out of MOS logic gates is very high because of their high input impedance.

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Logic Gates Families

- If any unused input terminal of a MOS gate is left unconnected, a large voltage may get induced at the unconnected input which may damage the gate.
- Different versions available in TTL logic gate family:
  - 74/54 L: Low-power
  - 74/54 H: High-power/High-speed
  - 74/54 LS: Low-power Schottky
  - 74/54 S: Schottky
  - 74/54 AS: Advanced Schottky
  - 74/54 ALS: Advanced Low-power Schottky.
- The supply voltage required for ECL logic family is 5.2V ± 10%
- Comparison of Different Logic Gate families

<table>
<thead>
<tr>
<th>Fan-out</th>
<th>DTL</th>
<th>TTL</th>
<th>ECL</th>
<th>CMOS</th>
<th>p-MOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Propagation Delay</td>
<td>30ns</td>
<td>10ns</td>
<td>40ns</td>
<td>70ns</td>
<td>300ns</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>8mw</td>
<td>10mw</td>
<td>40mw</td>
<td>0.01mw</td>
<td>0.2 – 10mw</td>
</tr>
<tr>
<td>Noise Margin (min.)</td>
<td>750mV</td>
<td>400mV</td>
<td>200mV</td>
<td>300mV</td>
<td>150mV</td>
</tr>
</tbody>
</table>

- Fastest logic gate family is ECL. It is also called Current Mode Logic.
- Slowest Logic gate family is CMOS.
- The logic gate family, which consumes less power CMOS.
- The logic gate family, which consumes more power ECL.
- The logic gate family, which is having highest fan out CMOS.
- In CMOS circuit p-MOS transistor conducts if the gate to source voltage is more positive whereas n-MOS conduct if gate to source voltage is more negative.
- NMOS is faster than PMOS.
- In tristate logic in addition to two low-impedance outputs 0 and 1, there is third state known as high impedance state.

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- Standard 2 input TTL NAND gate

2 - input NAND gate with Totem-pole output configuration

The Dido de 'D' is used to keep the transistor Q4 in OFF state when Q3 is in ON state.

2 - input NAND gate with open collector output configuration.

- Gates with open collector output can be used for wired-AND operation.

Wired-AND operation is equivalent to AND + OR + INVERT

Tristate output configuration - TTL circuit.

<table>
<thead>
<tr>
<th>Control input</th>
<th>A</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>X</td>
<td>Z</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

- NMOS gate circuits

NMOS gate with output + VDD

\[ Y = AB \]
• Similar to open collector output in TTL, open emitter outputs are available in ECL. The outputs of two or more ECL gates can be connected to get additional logic without using additional hardware. Wired - OR operation is possible with ECL gates.

\[ (A + B + C + D) = (A + B)(C + D) \]

• Wired - OR operation is equivalent to OR - AND - INVERT

• If any input of an ECL gate is left unconnected, the corresponding E - B junction will not be conducting. Hence it acts as if its logical 0 level voltage is applied to that input, i.e. in ECL ICs, all unconnected/ floating inputs are treated as logical OS.

Notes:
COMBINATIONAL DIGITAL CIRCUITS

POINTS TO REMEMBER:

1. Combinational digital circuits and
2. Sequential digital circuits.

Combinational Digital Circuits: These circuits "the outputs at any instant of time depends on the inputs present at that instance only."

For the design of Combinational digital circuits Basic gates (AND, OR, NOT) or universal gates (NAND, NOR) are used. Examples for combinational digital circuits are Half adder, Full adder, Half subtractor, Full subtractor, Code converter, Decoder, Multiplexer, Demultiplexer, Encoder, ROM, etc.

Sequential Digital Circuits: The outputs at any instant of time not only depends on the present inputs but also on the previous inputs or outputs.

For the design of these circuits in addition to gates we need one or more element flip-flop.

Examples for sequential digital circuits are Registers, Shift register, Counters etc.

Half adder: A combinational circuit that performs the addition of two bits is called a half adder. It consists of two inputs and two outputs.

\[
\begin{array}{c|c|c|c}
X & Y & \text{Carry} & \text{Sum} \\
0 & 0 & 0 & 0 \\
0 & 1 & 0 & 1 \\
1 & 0 & 0 & 1 \\
1 & 1 & 1 & 0 \\
\end{array}
\]

\[
\begin{array}{c|c|c|c}
X & Y & \text{Carry} & \text{Sum} \\
0 & 0 & 0 & 0 \\
0 & 1 & 1 & 1 \\
1 & 0 & 0 & 1 \\
1 & 1 & 1 & 0 \\
\end{array}
\]

Half Subtractor: It is a Combinational circuit that subtracts two bits and produces their difference, it also has an output to specify if a '1' has been borrowed.

\[
\begin{array}{c|c|c|c|c}
X & Y & \text{Borrow} & \text{Diff} \\
0 & 0 & 0 & 0 \\
0 & 1 & 1 & 1 \\
1 & 0 & 0 & 0 \\
1 & 1 & 1 & 0 \\
\end{array}
\]

Half adder can be converted into half subtractor with an additional inverter.

Quater Adder/Quater Subtract: The sum output of Half adder is called Quater adder. The difference output of Half subtractor is called Quater subtractor.

Quater Adder/Quater Subtract is used as two input XOR gate.

Full adder: It performs the addition of three bits (two significant bits and a previous carry) and generates sum and carry.

<table>
<thead>
<tr>
<th>X</th>
<th>Y</th>
<th>Z</th>
<th>Carry</th>
<th>Sum</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
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<td>0</td>
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<td>1</td>
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<td>0</td>
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<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Full adder can be implemented by using two half adders and an OR gate.

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Full subtractor:

Full subtractor can be implemented by using two half-subtractors and an OR gate.

Four bit binary parallel adder can be constructed by using three full adders and one half-adder or by using four full adders with input carry for least significant bit full adder is zero.

Four bit binary parallel adder shown in figure is also called Ripple carry adder.

Truth table of active high output type of decoder:

<table>
<thead>
<tr>
<th>X</th>
<th>Y</th>
<th>D0</th>
<th>D1</th>
<th>D2</th>
<th>D3</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>
Activate low output type of decoders will give the output low for given input combination and all other outputs are high.

Truth table of active high output type of decoder

<table>
<thead>
<tr>
<th>X</th>
<th>Y</th>
<th>D0</th>
<th>D1</th>
<th>D2</th>
<th>D3</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
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<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

- 3 to 8 line decoder is also called Binary-to-Octal decoder or converter. It is also called 1 of 8 decoder, because only one of the 8 outputs is activated at a time.

- Decoders are widely used in memory system of a computer where they respond to the address code input from the CPU to activate the memory storage location specified by the address code.

- Decoders are also used to convert binary data to a form suitable for displaying on decimal read outs.

- Decoders can be used to implement combinational circuits, Boolean functions etc.

- Demultiplexer: A decoder with enable input acts as a demultiplexer. A demultiplexer is a circuit that receives information on a single line and transmits that information on one of 2^n possible output lines. The selection of specific output line is controlled by the bit values of 'n' selection lines.

<table>
<thead>
<tr>
<th>E</th>
<th>A</th>
<th>B</th>
<th>D</th>
<th>D</th>
<th>D</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>X</td>
<td>X</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
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<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

- Multiplexers can be used for the implementation of Boolean functions, combinational circuits. They can also be used for parallel to serial conversion.

- Multiplexer is also called cell selector or universal element.

- All three-variable Boolean equations can be implemented by using 8 to 1 multiplexer without using any additional gates. Some but not all three-variable Boolean equations can also be implemented with 4 to 1 max without using any additional gates.

- Encoder: An encoder identifies a particular code present at the input terminals of the circuit. The inverse process is called Decoding. An Encoder has number of inputs (C) and only one of which is in the high state or active, and an n-bit code is generated upon which of the inputs is excited.

- ROM (Read Only Memory): ROM is nothing but the combination of decoder and Encoder. It is a semi-conductor memory and which is a permanent memory. ROM can also be defined as Simple Code conversion unit.

- The memory which is constructed by using only gates in ROM.
**POINT TO REMEMBER:**

- Two cross coupled inverters will form a basic latch which can store one bit of information.
- Flip-Flops: Flip-Flop is also called bistable multivibrator or binary. It can store one bit of information.
- In a flip-flop one output is always complement of the other output.
- Flip-Flop has two stable states.
- Clocked S-R Flip-Flop: It is called Set-Reset Flip-Flop.

<table>
<thead>
<tr>
<th>S</th>
<th>R</th>
<th>Q_{out}</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Q_{o}</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>*</td>
</tr>
</tbody>
</table>

**Truth table**

- The output of the flip-flop changes only during the clock pulse. In between clock pulses the output of the flip-flop does not change.

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- During normal operation of the flip-flop, preset and clear inputs must be always high.
- The disadvantage of S-R flip-flop is $S = 1$, $R = 1$ output cannot be determined. This can be eliminated in j-k flip-flop.
- S - R flip-flop can be converted to j-k flip-flop by using the two equations $S = JQ$ and $R = KQ$.

**Truth table**

- Race around problem is present in the j-k flip-flop, when both $J = K = 1$.
- Toggling the output more than once during the clock pulse is called Race around Problem.

- The Race around problem in J-K flip-flop can be eliminated by using edge triggered flip-flop or Master slave J-K flip-flop or by using the clock signal whose pulse width is less than or equal to the propagation delay of flip-flop.

- Master-slave flip-flop is a cascading of two J-K flip-flops Positive or direct clock pulses are applied to master and these are inverted and applied to the slave flip-flop.

- D-flip-flop: It is also called a Delay Flip-Flop. By connecting an inverter in between J and K input terminals, D flip-flop is obtained. K always receives the compliment of J.

**Truth table**

- D flip-flop is a binary used to provide delay. The bit on the D line is transferred to the output at the next clock pulse.
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If a K-1 flip-flop is connected with J and K terminals to a common point, then 

\[ Q_{n+1} = Q_n \]

This unit changes state of the output with each clock pulse and hence it acts as a toggle switch.

**Truth Table**

<table>
<thead>
<tr>
<th>D</th>
<th>J</th>
<th>K</th>
<th>Q_n</th>
<th>Q_{n+1}</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

If X kHz clock signal is applied to a T flip-flop when \( T = 1 \), then the output \( Q \) signal frequency is given by \( X/2 \) kHz. Thus it acts as a frequency divider.

**Synchronous Control inputs**

<table>
<thead>
<tr>
<th>Clock</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t )</td>
</tr>
<tr>
<td>( t' )</td>
</tr>
</tbody>
</table>

**Synchronous Control inputs**

<table>
<thead>
<tr>
<th>Clock</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t )</td>
</tr>
<tr>
<td>( t' )</td>
</tr>
</tbody>
</table>

Setup Time \( t_s \): Time interval immediately preceding the active transition of clock signal during which the control input must be maintained at the proper level.

**Hold Time \( t_H \):** The time interval immediately following the active transition of the clock signal during which the synchronous control input must be maintained at the proper level.

**Registers and Shift Registers:**

- A register is a group of flip-flops used to store binary information. An \( n \)-bit register can store \( n \) bits of information.

- A register which is able to shift the information either from left to right or from right to left is called a shift register.

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Sequential Digital Circuits

- **Shift register can perform four different operations.**
  1. **Serial input**
     - Parallel output.
  2. **Serial input**
     - Serial output.
  3. **Parallel input**
     - Parallel output.
  4. **Parallel input**
     - Serial output.

- **Universal Shift Register:** A register which is able to shift the information from left to right or from right to left and which can perform all four operations is called universal shift register.

- **Applications of Shift Registers:***
  1. Serial to parallel conversion (It is also called spatial to temporal code conversion).
  2. Parallel to serial conversion (It is also called temporal to spatial code conversion).
  4. Multiplication and Division.
  5. Ring counter and Twisted ring counter.
  6. Digital delay line (Serial input and serial output operations).

- **Left shift operation is nothing but multiplying by 2**.

\[
\begin{array}{c|c|c|c|c}
0 & 1 & 0 & 1 & 5 \\
1 & 0 & 1 & 0 & 10 \\
\end{array}
\]

Shift left by \( n \)-positions is equivalent to multiplication by \( 2^n \).

- If most significant bit is 0, then right shift operation by one position is same as Division by 2.

\[
\begin{array}{c|c|c|c|c}
1 & 0 & 1 & 0 & 5 \\
0 & 1 & 0 & 1 & 2 \\
\end{array}
\]

If \( L.S.B = 1 \), then shift right operation gives integer division by 2.

\[
\begin{array}{c|c|c|c|c|c}
0 & 1 & 0 & 1 & 5 \\
0 & 0 & 0 & 0 & 2 \\
\end{array}
\]

If 2.5

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COUNTERS:

- The Counter is driven by a clock signal and can be used to count the number of clock cycles. Counter is nothing but a frequency divider circuit.
- Two types of counters are available:
  1. Synchronous.
  2. Asynchronous.
- Synchronous counters are also called parallel counters. In this type of counters the clock pulses are simultaneously applied to all the flip-flops.
- Asynchronous counters are also called Ripple or serial counters. In this type of counters the output of one flip-flop is connected to the clock input of next flip-flop and so on.
- A counter having n-flip-flops can have $2^n$ output states i.e. it can count $2^n$ clock pulses (0 to $2^n-1$).
- The largest binary number that can be represented by an n-bit counter has a decimal equivalent of $(2^n-1)$. Example: n = 3, then $2^3 - 1 = 8 - 1 = 7$.
- A counter can be made to count either in the up mode or in the down mode.
- Synchronous counters are faster than asynchronous counters.
- The modulus of a counter is the total number of states through which the counter can progress. For example mod-8 counter is having 8 different states (000 to 111).
- The output signal frequency of Mod-n counter is $1/n$ of the input clock frequency. Hence the counter is also called $n$ counter.
- The number of flip-flops (n) required to construct Mod N counter can be obtained from the following formula:
  $$2^n \leq N$$
- A decade counter is also called Mod-10 or +10 counter requires 4 flip-flops.
- Any binary counter can be a modulus counter where as the modulus counter need not be a binary counter.
- Six flip-flops are required to construct mod-60 counter.

- Ring Counter: Shift register can be used as ring counter when Qn output terminal is connected to serial input terminal.
- An n-bit ring counter can have "n" different output states. It can count n-clock pulses.
- Twisted Ring counter: It is also called Johnson's Ring counter. It is formed when Qn output terminal is connected to the serial input terminal of the shift register.
- An n-bit twisted ring counter can have maximum of 2n different output states.

POINTS TO REMEMBER:

- The digital computer memory can be classified into two types: Primary memory or main memory and Secondary memory or Auxiliary memory.
- Primary memory or main memory: The memory, which is directly accessible to the CPU, is called main memory. Egs: ROM, RAM.
- Secondary memory or Auxiliary memory: The memory, which is not directly accessible to the CPU, is called secondary memory. Egs: Hard disk, Floppy disk, Magnetic tape etc.
- Primary memories are semiconductor memories. They are available in the form of integrated circuits with different memory capacities.
- The capacity of a memory IC is represented by $2^m$, where $2^m$ represents number of memory locations available and "m" represents number of bits stored in each memory location.
  Egs: $2^7 \times 8 = 1024 \times 8$.
- The number of address bits required to identify $2^n$ memory locations are "n".
  Egs: to identify one out of 1024 $(2^{10})$ memory locations, 10-address bits are required.
- Assigning addresses for different memory locations of a memory IC is called memory mapping.
- To increase the bit capacity or length of each memory location, the memory ICs are connected in parallel and the corresponding memory location of each IC must be selected simultaneously.
  Egs: 1024 X 8 memory capacity can be obtained by using four memory ICs of memory capacity 1024 X 2.
- To increase the number or memory locations (i.e. explanation of memory), the memory ICs are connected such that at any time only one memory IC must be selected.
  Egs: To get 4KX8 memory capacity, it is required to use four 1KX8 memory ICs, and at any time one of four memory ICs can be selected using a decoder.
- The number of memory ICs of capacity 1KX4 required to construct a memory of capacity 8K X 8 are 16.(i.e.16 memory ICs of 1KX4 capacity are required to construct 8KX8 memory).
Types of memories -

- Semiconductor memories
- Magnetic memories
  - Drum
  - Tape
  - Disk
  - Bubble
  - Core

Read / Write Memory
(RAM or user memory)

Read Only Memory
(ROM)

Static RAM
Dynamic RAM

PROM
EPROM
EAPROM (or) EEPROM

Memory device parameters or characteristics:

- **Access time:** The access time of a memory is defined as the time required to access a memory location for reading or writing.

- **Access rate:** It is defined as the reciprocal of access time. It is measured in words per second.

- **Access time:** It depends on the physical characteristics of the storage medium, and also on the type of access mechanism used.

- **Access mode:** An important property of a memory device is the order or sequence in which information can be accessed.

- **Random Access:** If the access time is independent of position of the memory location, then it is called random-access mode. E.g., ROM, CAM (content addressable memory)

- **Sequential Access:** A memory in which the locations can be accessed in a sequence only is referred to as sequential memory. E.g., Magnetic tape, magnetic bubble

---

Some memory devices such as magnetic disks or drums contain a large number of independent rotating tracks. If each track has its own read-write head, the tracks may be accessed randomly, although access within each track is serial. In such cases the access mode is sometimes called semi-random or direct access.

- **Alterability:** The method used to write information into a memory may not be irreversible. In that once information has been written, it can not be altered while the memory is in use i.e. on-line.

- **Memory whose contents can not be altered on-line** are called ROMs.

- **ROMs whose contents can be changed are called PROMs.**

- **Memories in which reading or writing can be done on-line are called R/W Memories.**

- **Volatile memory:** In this type of memory, the stored information is dependent on power supply. I.e., the stored information will remain as it is as long as power supply is applied. E.g., RAM.

- **Non-volatile memory:** In this type of memory, the stored information is independent of power supply. I.e., its stored information will persist as it is even if the power fails. E.g., ROM, P-ROM, E-PROM, etc.

- **PROM:** Programmable Read Only Memory
- **EPROM:** Erasable programmable Read Only Memory
- **EAPROM:** Electrically Alterable Programmable Read Only Memory

- **Static RAM (SRAM):** In this type of memory, binary information is stored in terms of voltage. SRAMs store ones and zeros using conventional Flip-flops.

- **Dynamic RAM (DRAM):** In this type of memory, binary information is stored in terms of charge on the capacitor. The memory cells of DRAMS are basically charge storage capacitors with three transistors. The presence or absence of charge in a capacitor is interpreted as logical 1 or 0.

- **Because of the leakage property of the capacitor, DRAMS require periodic charge refreshing to maintain data storage.**

- **The package density is more in the case of DRAMS. But additional hardware is required for memory refresh operation.**

- **SRAMS consume more power than DRAMS. SRAMS are faster than DRAMS.**

- **Erasable Read Only Memory:** The memory is known as erasable Read Only (ERO) memory if the reading method destroys its contents. For such memories each read operation must be followed by write operation to restore the contents. E.g., Magnetic Core.

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→ Non-destructive Read Out (NDRD): It is called NDRD if the reading operation does not change its contents. Ex: Magnetic tapes, disks, RAMs, ROMs, etc.

→ Semiconductor technologies used for fabrication of memories are:
   a) Bipolar and b) Unipolar (i.e. MOS)

→ CCD (charge coupled Device) is a volatile memory and sequential access-type.

→ Low-voltage and high access rates are desirable memory characteristics.

→ By changing the hardware logic used for the chip selection of memory IC, it is possible to change the memory mapping.

Notes:

Chapter – 8

A/D & D/A CONVERTERS

→ Digital to analog conversion needed in digital data processing requires translation of digital information to an equivalent analog information.

→ Digital to analog converters, may be used to translate the output of a digital system into an analog form for the purpose of driving a pen recorder or for a cathode-ray oscilloscope.

→ The D/A converter is commonly referred to as a decoding device, since it is used to decode the digital signals into proportional voltage or current signals for an entry into an analog system.

→ D/A converter converts digital information into corresponding analog signals.

→ There are two types of DAC’s are available:
   a) Binary weighted resister type of DAC and
   b) R-2R ladder type of DAC.

→ The R-2R ladder type of DAC is superior type of DAC.

→ Binary weighted resister type of DAC has many drawbacks.

→ When the number of input bits is large, the resistors used for LSB has to be very large value.

→ Each resister required in the network is of different value, as such the resistors used are to be chosen from wide range of values.

→ If each higher bit resister is not exactly half of the previous bit resister, the step size will change.

→ The advantage of R-2R ladder type of DAC over binary weighted resistor type of DAC:
   a) Better linearity and
   b) It requires only two different types of resistors with values R and 2R.

→ Linearity: A D/A converter is said to be ideally or perfectly linear, if it gives equal increments in the analog output voltage for equal increments in the numerical value of the digital value.

→ DA Resolution: It is defined as the smallest change in the analog output voltage corresponding to a change of one bit in the digital input.

→ The percentage resolution of an n-bit DAC is given by \[ \frac{1}{2^{n-1}} \times 100 \]
→ The resolution of an n-bit DAC with a range of output voltage from 0 to V volts is given by \( \frac{V}{2^n} \) Volts.

→ Settling time of DAC: It is defined as the time required for the analog output voltage to reach and stay within a specified limit, after application of a digital input.

→ Monotonicity: A DAC is said to be monotonic if its output voltage increases regularly as its binary digital input signal increases from one value to the next value. Output wave form should be perfectly staircase with no downward steps, as input is increased for a proper monotonic DAC.

→ The accuracy of a D/A converter is a measure of the difference between the actual analog output voltage and what the output should be in the ideal case.

→ An analog to digital converter ADC converts analog voltages into the corresponding digital code.

→ An ADC usually considered as an encoder.

→ The conversion time ADC is the time required for conversion of one analog sample to corresponding digital code.

→ Different types of ADC’s are available:
  → Simultaneous ADC or parallel comparator of Flash type of ADC
  → Counter type of ADC or pulse width type of ADC
  → Integrator type of ADC or single slope of ADC
  → Dual slope integrator ADC
  → Successive approximation type ADC etc.

→ Flash type of ADC is the fastest type of ADC

→ An n-bit Flash type of ADC requires \( 2^n - 1 \) comparators.

→ Counter type of ADC uses linear search and Successive approximation type of ADC uses binary search.

→ Ring counter is used in Successive approximation type of ADC.

→ ADC Resolution: It is defined as the change in the input voltage required for a one-bit change in the output.

Notes:

→ An ADC having an analog range of \(-V/2\) to \(+V/2\) and n-bit digital output has a resolution of \(V/(2^n - 1)\) volts.

→ Dual slope ADC is more accurate.

→ Flash type of ADC requires no counter.

→ Counter type of ADC and Successive approximation type of ADC used DAC.
4. The Boolean function realized by the logic circuit shown is

\[ F = \sum(0,1,3,5,7,8,10,14) \]

(a) \[ F = \sum(2,3,5,7,8,12,13) \]
(b) \[ F = \sum(2,3,5,7,8,9,13) \]

GATE-2009

5. The full forms of the abbreviations TTL and CMOS in reference to logic families are:

(a) Triode Transistor Logic and Chip Metal Oxide Semiconductor
(b) Tristate Transistor Logic and Chip Metal Oxide Semiconductor
(c) Transistor Transistor Logic and Complementary Metal Oxide Semiconductor
(d) Tri-state Transistor Logic and Complementary Metal Oxide Silicon

6. In a microprocessor, the service routine for a certain interrupt starts from a fixed location of memory which cannot be externally set, but the interrupt can be delayed or rejected. Such an interrupt is

(a) non - maskable and non - vectored
(b) maskable and non - vectored
(c) non - maskable and vectored
(d) maskable and vectored

7. If \( X = 1 \) in the logic equation

\[ (X + Z)(Y + (Z + XY)) \]

then

(a) \( Y = Z \)
(b) \( Y \neq Z \)
(c) \( Z = 1 \)
(d) \( Z = 0 \)

8. What are the minimum number of 2 to 1 multiplexers required to generate a 2-input AND gate and a 2-input XOR gate?

(a) 1 and 2
(b) 1 and 3
(c) 1 and 1
(d) 2 and 2
9. Refer to the NAND and NOR latches shown in the figure. The inputs \((P_1, P_2)\) for both the latches are first made \((0, 1)\) and then, after a few seconds, made \((1, 1)\). The corresponding stable outputs \((Q_1, Q_2)\) are:

- For the NAND latch: \((Q_1, Q_2) = (0, 0)\)
- For the NOR latch: \((Q_1, Q_2) = (0, 0)\)
- For the NOR latch: \((Q_1, Q_2) = (0, 0)\)
- For the NAND latch: \((Q_1, Q_2) = (0, 0)\)

10. What are the counting states \((Q_1, Q_2)\) for the counter shown in the figure below?

(a) 11, 10, 00, 11, 10,...
(b) 01, 10, 11, 00, 01,...
(c) 00, 11, 01, 10, 00,...
(d) 01, 10, 00, 01, 10,...

Statement for Linked Answer Questions 11 and 12.

Two products are sold from a vending machine, which has two push buttons \(P_1\) and \(P_2\). When a button is pressed, the price of the corresponding product is displayed in a 7-segment display.

If no buttons are pressed, "0" is displayed, signifying "No Command".

11. If only \(P_1\) is pressed, "2" is displayed, signifying "Rs. 2."

12. If only \(P_2\) is pressed, "5" is displayed, signifying "Rs. 5."

If both \(P_1\) and \(P_2\) are pressed, "E" is displayed, signifying "Error".

The names of the segments in the 7-segment display, and the glow of the display for '0', '2', '5' and 'E' are shown below.

(i) push button pressed/not pressed is equivalent to logic 1/0 respectively
(ii) a segment glowing/not glowing in the display is equivalent to logic 1/0 respectively.

Consider:

(i) push button pressed/not pressed is equivalent to logic 1/0 respectively
(ii) a segment glowing/not glowing in the display is equivalent to logic 1/0 respectively.

11. If segments a to g are considered as functions of \(P_1\) and \(P_2\) then which of the following is correct?

(a) \(g = P_1 \oplus P_2\)
(b) \(g = P_1 \land P_2\)
(c) \(g = P_1 \land P_2\)
(d) \(g = P_1 \lor P_2\)

12. What are the minimum numbers of NOT gates and 2-input OR gates required to design the logic of driver for this 7-segment display?

(a) 3 NOT and 4 OR
(b) 2 NOT and 4 OR
(c) 1 NOT and 3 OR
(d) 2 NOT and 3 OR

GATE-2008

13. The logic function implemented by the following circuit at the terminal OUT is:

(a) \(P \oplus Q\)
(b) \(P \land Q\)
(c) \(P \land Q\)
(d) \(P \land Q\)
14. The two numbers represented in signed 2’s complement form are \( P = 1110101 \) and \( Q = 11100110 \). If \( Q \) is subtracted from \( P \), the value obtained in signed 2’s complement form is:
   (a) 00000110 (b) 00000111 (c) 1111101 (d) 11111101

15. Which of the following Boolean Expressions correctly represents the relation between \( P, Q, R \) and \( M_i \)?
   (a) \( M_i = (PR\ OR\ Q)\ XOR\ R \)
   (b) \( M_i = (PR\ AND\ Q)\ XOR\ R \)
   (c) \( M_i = (PR\ OR\ Q)\ XOR\ R \)
   (d) \( M_i = (PR\ XOR\ Q)\ XOR\ R \)

16. For the circuit shown in the following figure, \( I_1 \) to \( I_6 \) are inputs to the 4:1 multiplexer. \( R \) (MSB) and \( S \) are control bits.

   - The output \( Z \) can be represented by
     - \( P \overline{Q} + P Q S + \overline{Q} R S \)
     - \( P \overline{Q} + P Q \overline{E} + \overline{P} Q S \)
     - \( P \overline{Q} R + P Q R + P Q R S + \overline{Q} R S \)
     - \( P Q R + P Q R S + P Q R S + Q R S \)

17. For each of the positive edge-triggered J-K Flip flop used in the following figure, the propagation delay in \( \Delta T \)

   Which of the following waveforms correctly represents the output at \( Q \)?
   (a) ![Waveform A](image)
   (b) ![Waveform B](image)
   (c) ![Waveform C](image)
   (d) ![Waveform D](image)

18. For the circuit shown in the figure, \( D \) has a transition from 0 to 1 after \( CLK \) changes from 1 to 0. Assume gate delays to be negligible.

   Which of the following statements is true?
   (a) \( Q \) goes to 1 at the \( CLK \) transition and stays at 1.
   (b) \( Q \) goes to 0 at the \( CLK \) transition and stays at 0.
   (c) \( Q \) goes to 1 at the \( CLK \) transition and goes to 0 when \( D \) goes to 1.
   (d) \( Q \) goes to 0 at the \( CLK \) transition and goes to 1 when \( D \) goes to 1.
Statement for linked answer questions:

In the Digital-to-Analog converter circuit shown in the figure below, \( V_S = 10 \, \text{V} \) and \( R = 10 \, \text{k}\Omega \)

28. The current is
   (a) 31.25 \, \mu\text{A}  (b) 62.5 \, \mu\text{A}  (c) 125 \, \mu\text{A}  (d) 250 \, \mu\text{A}

29. The Voltage \( V_D \) is
   (a) 0.781 \, \text{V}  (b) 1.562 \, \text{V}  (c) 3.125 \, \text{V}  (d) 6.250 \, \text{V}

30. The Circuit diagram of a standard TTL NOT gate is shown in the figure. When \( V_I = 2.5 \, \text{V} \), the modes of operation of the transistors will be

   (a) \( Q_1 \) : reverse active; \( Q_2 \) : normal active; \( Q_3 \) : saturation; \( Q_4 \) : cut-off
   (b) \( Q_1 \) : reverse active; \( Q_2 \) : saturation; \( Q_3 \) : saturation; \( Q_4 \) : cut-off
   (c) \( Q_1 \) : normal active; \( Q_2 \) : cut-off; \( Q_3 \) : cut-off; \( Q_4 \) : saturation
   (d) \( Q_1 \) : saturation; \( Q_2 \) : saturation; \( Q_3 \) : saturation; \( Q_4 \) : normal active

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31. The number of product terms in the minimized SOP expression obtained through the following K-map is (where, 'X' denotes don't care states)

   (a) 2  (b) 3  (c) 4  (d) 5

   \[ \begin{array}{cccc}
   & 0 & 1 & X \\
   0 & 1 & 0 & 1 \\
   1 & 0 & 1 & X \\
   \end{array} \]

32. A new Binary Coded Pentary (BCP) number system is proposed in which every digit of a base-5 number is represented by its corresponding 3-bit binary code. For example, the base-5 number 24 will be represented by its BCP code 110100. In this numbering system, the BCP code 100010011001 corresponds to the following number is base-5 system

   (a) 425  (b) 1324  (c) 2201  (d) 4231

33. For the circuit shown in the figure below, two 4-bit parallel in-serial-out shift registers loaded with the data shown are used to feed the data to a full adder, initially, all the flip-flops are in clear state. After applying two clock pulses, the outputs of the full adder should be

   (a) \( S=0 \, C_4=0 \)
   (b) \( S=0 \, C_4=1 \)
   (c) \( S=1 \, C_4=0 \)
   (d) \( S=1 \, C_4=1 \)

34. A 4-bit D/A converter is connected to a free-running 3-bit UP counter, as shown in the following figure, which of the following waveforms will be observed at \( V_O \)?

   (a) \[ \text{Waveform A} \]
   (b) \[ \text{Waveform B} \]
   (c) \[ \text{Waveform C} \]
   (d) \[ \text{Waveform D} \]

In the figure shown above, the ground has been shown by the symbol

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\[ www.raghul.org \]
35. Two D-flip-flops, as shown below, are to be connected as a synchronous counter that goes through the following sequence: 00 → 01 → 11 → 10 → 00
The inputs D3 and D2, respectively should be connected as:

(a) Q3 and Q2
(b) Q1 and Q0
(c) Q2 and Q1
(d) Q0
36. The point P in the following figure is stuck-at-1. The output f will be:

(a) ABC
(b) A
(c) AB′C
(d) A′A

37. Decimal 43 is hexadecimal and BCD number system is respectively
(a) B3, 01000011
(b) 2B, 01000011
(c) 32, 00110100
(d) BS, 01001100

38. The Boolean function f implemented in the figure using two input multiplexers is:

(a) ABC + AB′C
(b) ABC + AB′C
(c) ABC + AB′C
(d) ABC + AB′C

39. The transistors used in the operation of the TTL gate shown in the figure have a β = 100. The base-emitter voltage of is 0.7 V for a transistor in active region and 0.7 V for a transistor in saturation. If the sink current I_s = 1 mA and the input is at logic 0, then the current I_k will be equal to:

(a) 0.65 mA
(b) 0.70 mA
(c) 0.75 mA
(d) 1.00 mA

40. The Boolean expression for the truth table shown is:

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>f</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

(a) B (A + C) (A + C)
(b) B (A + C) (A + C)
(c) B (A + C) (A + C)
(d) B (A + C) (A + C)

41. Both transistors T1 and T2 show in the figure, have a threshold voltage of 1 Volt. The device parameters K1 and K2 of T1 and T2 are, respectively, 36 µA/V^2 the output voltage V_y is:

(a) 3V
(b) 2V
(c) 3V
(d) 4V
42. The present output $Q_3$ of an edge triggered JK flip-flop is logic 1. If $J=1$, then $Q_{3+1}$ is (a) cannot be determined (b) will be logic 0 (c) will be logic 1 (d) will race around

43. The given figure shows a ripple counter using positive edge triggered flip-flops. If the present state of the counter is $Q_2$ Q_1 Q_0 = 011, then its next state ($Q_2$ Q_1 Q_0) will be

(a) 010  (b) 100  (c) 111  (d) 101

GATE-2004

44. The range of signed decimal numbers that can be represented by 6-bit 1's complement number is

(a) -63 to +63  (b) -63 to +63  (c) -64 to +63  (d) -32 to +31

45. The figure shown the internal schematic of a TTL AND-OR-Invert (AOI) gate. For the inputs shown in the figure, the output $Y$ is

(a) 0  (b) 1  (c) AB  (d) AB

46. The minimum number of 2-to-1 multiplexers required to realize 4-to-1 multiplexor is

(a) 1  (b) 2  (c) 3  (d) 4

47. The Boolean expression $AC + BC$ is equivalent to

(a) $AC + BC + AC$  (b) $BC + AC + BC + ABC$  (c) $AC + BC + BC + ABC$  (d) $ABC + ABC + ABC + ABC$

48. 311001, 10011 and 110010 correspond to the 2's complement representation of which one of the following sets of numbers?

(a) 25, 9 and 57 respectively (b) -6, -5 and -6 respectively (c) -7, -7 and -7 respectively (d) -25, -9 and -57

Notes:

49. In the module -6 ripple counter shown in the figure, the output of the 2-input gate is used to clear the 3-K flip-flop

The 2-input gate is

(a) a NAND gate  (b) a NOR gate  (c) an OR gate  (d) an AND gate

50. A Boolean function $f$ of two variables $x$ and $y$ is defined as follows: $f(0,0) = 0, f(0,1) = f(1,1) = 1; f(1,0) = 0$

Assuming complements of $x$ and $y$ are not available, a minimum cost solution for realizing $f$ using only 2-input NOR gates and 2-input OR gates (each having unit cost) would have a total cost of

(a) 1 unit  (b) 4 unit  (c) 3 unit  (d) 2 unit

GATE-2003

51. The circuits shown in the figure has 4 boxes each described by inputs $P$, $Q$, $R$ and outputs $Y$, $Z$ with $Y = P \oplus Q \oplus R$; $Z = BQ + FR + QP$

(a) 4 bit adder giving $P + Q$  (b) 4 bit subtractor giving $P - Q$  (c) 4 bit subtractor giving $Q - P$  (d) 4 bit adder giving $P + Q + R$

52. A 4 bit ripple counter and a 4 bit synchronous counter are made using flip flops having a propagation delay of 10 ns each. If the worst case delay in the ripple counter and the synchronous counter be R and S respectively, then

(a) $R = 10ns$, $S=40ns$  (b) $R=40ns$, $S=10ns$  (c) $R=10ns$, $S=30ns$  (d) $R=30ns$, $S=10ns$
53. If the functions W, X, Y and Z are as follows:

\[ W = R \cdot \overline{Q} \cdot \overline{P} + \overline{R} \cdot S \]
\[ X = \overline{P} \cdot \overline{R} + P \cdot \overline{R} + S \cdot \overline{P} + S \cdot R \]
\[ Y = R \cdot S + P \cdot \overline{R} + P \cdot S + \overline{P} \cdot S \]
\[ Z = \overline{R} \cdot S + \overline{Q} \cdot R + \overline{P} \cdot \overline{Q} \cdot \overline{R} \cdot \overline{S} \]

Then

(a) \( W = Z \), \( X = Z \), \( X = Y \)
(b) \( W = Z \), \( X = Y \)
(c) \( W = Y \)
(d) \( W = Y - Z \)

54. The DTL, TTL, ECL and CMOS and families of digital ICs are compared in the following 4 columns:

<table>
<thead>
<tr>
<th>Family</th>
<th>ECL</th>
<th>DTL</th>
<th>TTL</th>
<th>CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage level</td>
<td>5V</td>
<td>3V</td>
<td>5V</td>
<td>3V</td>
</tr>
<tr>
<td>Propagation delay (ns)</td>
<td>10</td>
<td>20</td>
<td>30</td>
<td>40</td>
</tr>
<tr>
<td>Power consumption (mA)</td>
<td>100</td>
<td>50</td>
<td>30</td>
<td>20</td>
</tr>
</tbody>
</table>

The correct column is

(a) P
(b) Q
(c) R
(d) S

55. The circuit shown in the figure is a 4 bit DAC

The input bits 0 and 1 are represented by 0 and 5 V respectively. The OP AMP is ideal, but all the resistances and the 5 V inputs have a tolerance of ±10%. The specification (rounded to the nearest multiple of 5%) for the tolerance of the DAC is

(a) ±5%
(b) ±10%
(c) ±10%
(d) ±15%

56. The circuit shown in the figure converts

(a) BCD to binary code
(b) Binary to excess – 3 code
(c) Excess-3 to Gray code
(d) Gray to binary code

Notes:

57. In the circuit shown in the figure, A parallel-in, parallel-out 4 bit register, which load at the rising edge of the clock C. The output lines are connected to a 6 bit bus, W. Its output has as the input to a 10X4 ROM whose output is floating when the enable input E is 0. A partial table of the contents of the ROM is as follows:

<table>
<thead>
<tr>
<th>Address</th>
<th>0</th>
<th>1</th>
<th>2</th>
<th>4</th>
<th>6</th>
<th>8</th>
<th>10</th>
<th>12</th>
<th>14</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data</td>
<td>01</td>
<td>11</td>
<td>00</td>
<td>00</td>
<td>11</td>
<td>01</td>
<td>00</td>
<td>00</td>
<td>00</td>
</tr>
</tbody>
</table>

The clock to the register is shown, and the data on the W bus at time \( t_1 \) is \( \text{0110} \). The data on the bus at time \( t_2 \) is

(a) \( \text{1111} \)
(b) \( \text{1011} \)
(c) \( \text{1000} \)
(d) \( \text{0010} \)

GATE-2002

58. 4-bit 2's complement representation of a decimal number is 1000, the number is

(a) +8
(b) 0
(c) -7
(d) -8

59. In a number of comparators required in a 3-bit comparator type ADC is

(a) 2
(b) 3
(c) 7
(d) 8

Notes:
60. If the input to the digital circuit (in the figure) consisting of a cascade of 20 XOR-gates is \( X \), then the output \( Y \) is equal to

(a) 0  
(b) 1  
(c) \( \bar{X} \)  
(d) X

61. The gates \( G_1 \) and \( G_2 \) in the figure have propagation delay of 10 nsec and 20 nsec respectively. If the input \( V_i \) makes an abrupt change from logic 0 to 1 at time \( t=0 \), then the output wave from \( V_o \) is

(a)  
(b)  
(c)  
(d)  

62. The circuit in the figure has two CMOS NOR-gates. This circuit functions as:

(a) Flip-Flop  
(b) Schmitt trigger  
(c) Monostable multivibrator  
(d) Astable multivibrator

Notes:

63. If the input \( X_1, X_2, X_3, X_4 \) to the ROM in the figure are \( 0, 4, 2, 1 \) BCD numbers, then the output \( Y_3, Y_2, Y_1, Y_0 \) are:

(a)  
(b)  
(c)  
(d)  

64. The 2's complement representation of \( -17 \) is

(a) 1011  
(b) 10111  
(c) 111110  
(d) 110001

65. For the ring oscillator shown in the figure, the propagation delay of each inverter is 100 pico sec. What is the fundamental frequency of the oscillator output?

(a) 10MHz  
(b) 100MHz  
(c) 1 GHz  
(d) 2 GHz

66. In the figure, the LED

(a) emits light when both \( S_1 \) and \( S_2 \) are closed.  
(b) emits light when both \( S_1 \) and \( S_2 \) are open.  
(c) emits light when only \( S_1 \) is closed.  
(d) does not emit light, irrespective of the switch positions.
67. In the TTL circuit in the figure, $S_0$ to $S_4$ are select lines and $X_0$ to $X_4$ are input lines, $S_0$ and $X_0$ are LSBs. The output $Y$ is

(a) indeterminate
(b) $AB + A'B$
(c) $A + B$
(d) $C + A + B$ $C(A + B)$

68. The digital block in the figure is realized using two positive edge triggered D-flip-flops. Assume that for $T=0$, $Q_1 = Q_2 = 0$. The circuit in the digital block is given by:

(a) $X$
(b) $Y$
(c) $Z$
(d) $W$

69. In the DRAM cell in the figure, the $V1$ of the N-type MOSFET is 1V. For the following three combinations of $WL$ and $BL$, voltages:
(a) 5V; 3V; 7V
(b) 4V; 3V; 4V
(c) 5V; 5V; 3V
(d) 4V; 4V; 4V

70. For the logic circuit shown in the figure, the required input condition $(A, B, C)$ to make the output $(Y) = 1$ is

(a) $1, 0, 1$
(b) $0, 0, 1$
(c) $1, 1, 1$
(d) $0, 1, 1$

71. For the logic circuit shown in the figure, the simplified Boolean expression for the output $Y$ is

(a) $(A + B + C)$
(b) $A$
(c) $B$
(d) $C$

72. For the 4 bit DAC shown in the figure, the output voltage $V_o$ is

(a) 10V
(b) 4V
(c) 8V
(d) 6V

73. A sequential circuit using D-flip-flop and logic gates is shown in the figure, where $X$ and $Y$ are the inputs and $Z$ is the output. The circuit is:

(a) S-R Flip-flop with inputs $X = R$ and $Y = S$
(b) S-R Flip-flop with inputs $X = S$ and $Y = R$
(c) J-K Flip-flop with inputs $X = J$ and $Y = K$
(d) J-K Flip-flop with inputs $X = K$ and $Y = J$
74. In the figure, the J and K inputs of all the four Flip-Flops are made high. The frequency of the signal at output Y is

(a) 1.0 KHz
(b) 0.91 KHz
(c) 0.53 KHz
(d) 0.77 KHz

KEY

1. a 2. d 3. a 4. d 5. c 6. e 7. d 8. a
17. b 18. c 19. 20. 21. c 22. d 23. b 24. a
25. b 26. c 27. a 28. b 29. 30. a 31. a 32. a
33. a 34. b 35. a 36. d 37. b 38. a 39. c 40. a
41. a 42. c 43. b 44. b 45. a 46. c 47. d 48. c
49. a 50. a 51. b 52. b 53. a 54. b 55. a 56. a
57. a 58. a 59. c 60. a 61. b 62. c 63. b 64. b
65. a 66. a 67. b 68. a 69. b 70. d 71. b 72. b
73. d 74. b

Related Answer Questions

Statements for linked Answer questions 2 and 3

The following Karnaugh map represents a function F.

\[ F = \begin{cases} 0 & 1 \end{cases} \]

2. A minimized form of the function F is
   (A) \( F = XY + YZ \)
   (B) \( F = X + YZ \)
   (C) \( F = X + YZ \)
   (D) \( F = XY + YZ \)

3. Which of the following circuits is a realization of the above function F?

\[ \begin{align*}
\text{Option A} & \quad \text{Option B} \\
\text{Option C} & \quad \text{Option D}
\end{align*} \]
GATE – 2009

4. The increasing order of speed of data access for the following devices is
   (i) Cache Memory
   (ii) CD-ROM
   (iii) Dynamic RAM
   (iv) Processor Registers
   (v) Magnetic Tape
   (A) (v), (ii), (iii), (iv), (i)
   (B) (v), (ii), (iii), (i), (iv)
   (C) (ii), (i), (iii), (iv), (v)
   (D) (v), (ii), (i), (iii), (iv)

5. The complete set of only those Logic Gates designated as Universal Gates is
   (A) NOT, OR, and AND Gates
   (B) XOR, NOR and NAND Gates
   (C) NOR and NAND Gates
   (D) XOR, NOR and NAND Gates

GATE – 2007

07. A, B, C and D are input bits, and Y is the output bit in the XOR gate circuit of the figure below. Which of the following statements about the sum S of A, B, C, D and Y is correct?
   (A) S is always either zero or odd
   (B) S is always either zero or even
   (C) S = 1 only if the sum of A, B, C and D is even
   (D) S = 1 only if the sum of A, B, C and D is odd

GATE – 2006

08. A TTL NOT gate circuit is shown in figure. Assuming $V_{cc} = 5.0$ V of both the transistors, if $V_{i} = 3.0$ V, then the state of the two transistors, will be
   (A) $Q_{1}$ ON and $Q_{2}$ OFF
   (B) $Q_{1}$ reverse ON and $Q_{2}$ OFF
   (C) $Q_{1}$ reverse ON and $Q_{2}$ ON
   (D) $Q_{1}$ OFF and $Q_{2}$ reverse ON
9. A 4 x 1 MUX is used to implement a 3-input Boolean function as shown in figure. The Boolean function \( F(A, B, C) \) implemented is

\[
F(A, B, C) = \begin{cases} 
1 & \text{if } A \oplus B \oplus C \\
0 & \text{otherwise}
\end{cases}
\]

(A) \( F(A, B, C) = 2(1, 2, 4, 6) \)
(B) \( F(A, B, C) = 2(1, 7, 6) \)
(C) \( F(A, B, C) = 2(2, 4, 5, 6) \)
(D) \( F(A, B, C) = 2(1, 5, 6) \)

GATE - 2005

10. Select the circuit which will produce the given output \( Q \) for the input signals \( X_1 \) and \( X_2 \) given in the figure.

11. A digital-to-analog converter with a full-scale output voltage of 3.3 V has a resolution close to 14 mV. Its bit size is

(A) 4  
(B) 8  
(C) 16  
(D) 32

12. If \( X_1 \) and \( X_2 \) are the inputs to the circuit shown in the figure, the output \( Q \) is

(A) \( X_1 + X_2 \)  
(B) \( X_1 \cdot X_2 \)  
(C) \( X_1 + X_2 \)  
(D) \( X_1 \cdot X_2 \)

13. The digital circuit shown in the figure works as a

(A) JK flip-flop  
(B) Clocked RS flip-flop  
(C) T flip-flop  
(D) Ring oscillator

14. In the figure, as long as \( X_1 = 1 \) and \( X_2 = 1 \), the output \( Q \) remains

(A) at 1  
(B) at 0  
(C) at its initial value  
(D) unstable

GATE - 2004

15. The digital circuit using two inverters shown in fig. will act as

(A) a bistable multi-vibrator  
(B) an astable multi-vibrator  
(C) a monostable multi-vibrator  
(D) an oscillator

16. The simplified form of the Boolean expression \( Y = (A \cdot B \cdot C) + \overline{A \cdot B} \cdot \overline{C} \cdot \overline{D} \) can be written as

(A) \( A \cdot B + C \cdot D \)  
(B) \( A \cdot D + B \cdot C \cdot D \)  
(C) \( A \cdot B + \overline{C} \cdot \overline{D} \)  
(D) \( A \cdot B + B \cdot C \cdot D \)
17. A digital circuit which compares two numbers \(A_1 A_2 A_3\) \(A_4 \) \(A_5 \) \(A_6 \) \(A_7 \) \(A_8 \) \(B_1 B_2 B_3 B_4 B_5 B_6 B_7 B_8\) is shown in fig. To get output \(Y = 0\), choose one pair of correct input numbers.

(A) 1010, 1010
(B) 0101, 0101
(C) 0010, 0010
(D) 0100, 1011

18. The digital circuit shown in fig. generates a modified clock pulse at the output. Choose the correct output waveform from the options given below.

19. Fig. shows a 4-to-1 MUX to be used to implement the sum \(S\) of a 1-bit full adder with input bits \(P\) and \(Q\) and the carry input \(C_{in}\). Which of the following combinations of inputs to \(A_1\), \(A_2\), \(A_3\) and \(A_4\) of the MUX will realize the sum \(S\)?

(A) \(A_2 = A_4 = A_3 = A_1 = C_{in}\)
(B) \(A_2 = A_3 = A_1 = A_4 = C_{in}\)
(C) \(A_2 = A_1 = A_3 = A_4 = C_{in}\)
(D) \(A_2 = A_1 = A_4 = A_3 = C_{in}\)

20. The Boolean expression

\[ XYZ + XYZ + XYZ + XYZ \]

can be simplified to

(A) \(X\overline{Z} + \overline{X} + Y \overline{Z}\)
(B) \(XZ + \overline{Y} \overline{Z} + Y \overline{Z}\)
(C) \(XY + Z + XZ\)
(D) \(X \overline{Y} + \overline{X} + \overline{Z}\)

GATE – 2003

21. The shift register shown in fig. is initially loaded with the bit pattern 1010. Subsequently the shift register is clocked, and with each clock pulse the output bit is shifted by one bit position to the right. With each shift, the bit at the serial input is placed to the left most position (msb). After \(4\) clock pulses will the content of the shift register become 1010 again?

(A) 3
(B) 7
(C) 11
(D) 15

22. An X-Y flip flop, whose Characteristic Table is given below is to be implemented using a J-K flip flop

<table>
<thead>
<tr>
<th>(Q_{n+1})</th>
<th>(Q_n)</th>
<th>(J)</th>
<th>(K)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

This can be done by making

(A) \(J = X, K = \overline{Y}\)  \(\quad\) (B) \(J = \overline{X}, K = Y\)
(C) \(J = Y, K = \overline{X}\)  \(\quad\) (D) \(J = \overline{Y}, K = X\)

GATE – 2002

23. For the circuit shown in Fig. P2.10, the Boolean expression for the output \(Y\) in terms of inputs \(P, Q, R\) and \(S\) is

(A) \(P + Q + R + S\)
(B) \(P + Q + R + S\)
(C) \((P + Q)(R + S)\)
(D) \((P + Q)(R + S)\)

GATE – 2002

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24. The ripple counter shown in fig. is made up of negative edge triggered J-K flip-flops. The signal levels at J and K inputs of all the flip-flops are maintained at logic1. Assume that all outputs are cleared just prior to applying the clock signal.

(A) Create a table of Q0, Q1, Q2 and A in the format given below for 10 successive input cycles of the clock CLK.

(B) Determine the module number of the counter.

(C) Modify the circuit of fig. to create a modulo-6 counter using the same components used in the figure.

Format for (A): 

\[ \text{CLK} \quad Q_0 \quad Q_1 \quad Q_2 \quad A \]

---

GATE – 2001

25. The output f of the 4-to-1 MUX shown in fig. is

(A) \( xy + x \)

(B) \( x + y \)

(C) \( x \cdot y \)

(D) \( xy + x \)

---

26. For the ring counter shown in fig., find the steady state sequence if the initial state of the counter is 1110(c.e., Q3 Q2 Q1 Q0 = 1110). Determine the MOD number of the counter.

---

GATE – 2000

27. The minimal product-of-sums function described by the K-map given in Fig.P1.4.

(A) \( A'C' \)

(B) \( A' + C \)

(C) \( A + C \)

(D) \( AC \)

28. The counter shown in fig. is initially in state Q3 = 0, Q2 = 1, Q1 = 0. With reference to the CLK input, draw waveforms for Q0, Q1, Q2 and P for the next three CLK cycles.

---

GATE – 1999

29. For a flip-flop formed from two NAND gates as shown in the figure. The unstable state corresponds to

(A) \( X = 0, Y = 0 \)

(B) \( X = 0, Y = 1 \)

(C) \( X = 1, Y = 0 \)

(D) \( X = 1, Y = 1 \)

---

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30. The logic function \( F = \overline{A} \cdot \overline{B} \cdot \overline{C} + \overline{A} \cdot \overline{C} + \overline{A} \cdot \overline{D} \) is to be realized using an 8 to 1 multiplexer shown in the figure, using \( A, C \) and \( D \) as control inputs.

(a) Indicate the inputs to be applied at the terminals 0 to 7.
(b) Can the function be realized using a 4 to 1 multiplexer?

GATE – 1998

31. The open collector outputs of two 2-input NAND gates are connected to a common pull up resistor. If the input to the gates are \( P, Q \) and \( R, S \) respectively, the output is equal to:

(A) \( P \cdot Q \) \( R \cdot S \)
(B) \( P \cdot Q + R \cdot S \)
(C) \( P \cdot Q + R \cdot S \)
(D) \( P \cdot Q + R \cdot S \)

32. In standard TTL gates, the totem pole output stage is primarily used to:

(A) Increase the noise margin of the gate
(B) Decrease the output switching delay
(C) Facilitate a wired OR logic connection
(D) Increase the output impedance of the circuit

33. (a) Construct the truth table for the circuit given in Figure 1. \( Q_1 \), \( Q_2 \), and \( Q_3 \) are outputs and the clock pulse is the input. Unused J/K inputs are assumed to be at 0.
(b) Sketch the output waveforms of \( Q_1, Q_2 \), and \( Q_3 \).
(c) What function does this circuit perform?

---

ACE Academy
GATE Examination Questions

GATE – 1997

34. A 3-input 2-output priority encoder has the following truth table where \( X \)'s indicate don't care conditions. Realize the logic using NAND gates and inverters.

<table>
<thead>
<tr>
<th>( W_1 )</th>
<th>( W_2 )</th>
<th>( Y_1 )</th>
<th>( Y_2 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>( X )</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>( X )</td>
<td>( X )</td>
<td>1</td>
</tr>
</tbody>
</table>

GATE – 1996

35. The Boolean expression for the output of the logic circuit shown in Figure is

(A) \( Y = \overline{A} + \overline{B} + \overline{C} \)
(B) \( Y = A + B + C \)
(C) \( Y = \overline{A} \cdot B + \overline{A} \cdot C \)
(D) \( Y = A \cdot B + A \cdot C \)

KEY

| 1a 2b 3d 4a 5c 6d 7d 8c |
| 9a 10d 11b 12c 13a 14d 15c 16a |
| 17d 18b 19c 20b 21b 22b 23b 24a |
| 25b 26a 27a 28a 29d 30a 31b 32b |
| 33a 34a 35b |

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Chapter 9

INTRODUCTION TO MICROPROCESSORS

BASICS:

> Digital Computer: A programmable machine that processes binary data. It is traditionally represented by five blocks: Arithmetic Logic Unit (ALU), Control Unit, Memory, Input Unit and Output Unit.

> Central Processing Unit (CPU): The group of circuits that processes data and provides control signals and timing. It includes ALU, Control Unit and a group of registers.

> ALU: The group of circuits that performs arithmetic and logic operations. The ALU is a part of CPU.

> Control Unit: The group of circuits that provides timing and signals to all operations in the computer and controls the data flow.

> Memory: A medium that stores binary information.

> Input: It is a device that transfers information from the outside world to the computer.

> Output: It is a device that transfers information from the computer to the outside world.

> Microprocessor: A microprocessor is a semiconductor device which is manufactured by using LSI or VLSI technology, which includes ALU, Control Unit and a group of Registers in a single integrated circuit.

> Microcontroller: It is a device that includes microprocessor, memory, and simple I/O Interface logic on a single chip, fabricated using VLSI technology.

> Bit: Binary Digit.

> Nibble: A group of four bits is called a nibble.

> Byte: A group of eight bits is called a byte.

> Word: A group of bits the computer recognizes and processes at a time.

> Instruction: A command in binary that is recognized and executed by the computer to accomplish a task.

> Mnemonic Instruction: A meaningful combination of letters used to suggest the operation of an instruction.

> Bus: A group of wires or lines used to transfer data between the microprocessor and other components of the computer system. Or a path used to carry signals, such as connection between memory and the CPU in a digital computer.

> Bit capacity of a microprocessor: It is defined as the number of bits it can process at a time in parallel. For example, an 8-bit microprocessor can perform all 8-bit operations.

> In general, the internal architecture of the microprocessor depends on the bit capacity of the microprocessor.

> The system bus of the microcomputer consists of three types of buses: Address Bus, Data Bus and Control Bus.

> Address Bus: A group of lines that are used to send a memory address or a device address from the Microprocessor Unit (MPU) to the memory or the peripheral. The address bus is always unidirectional. Address always goes out of the microprocessor.

> The addressing capacity of any microprocessor is given by 2^n, where 'n' is nothing but the number of address lines available to the microprocessor.

> Data Bus: A group of lines used to transfer data between the MPU and peripherals (or memory). The data bus is always bi-directional.

> In general, the width of the data bus is equal to the bit capacity of the microprocessor.

> In general, the internal architecture of the microprocessor depends on the data bus width.

> Control Bus: The single lines that are generated by the MPU to provide timing of various operations.

> Intel Corporation introduced the first microprocessor in 1971. Its bit capacity was 4.

$\text{SV Rao}$

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### Microprocessors

Some of the example microprocessors are given below:

<table>
<thead>
<tr>
<th>Name</th>
<th>Word Length Memory</th>
<th>Addressing Capacity</th>
<th>Number Of Pins</th>
<th>Number Of Transistors</th>
</tr>
</thead>
<tbody>
<tr>
<td>4004</td>
<td>4-bit</td>
<td>640 bytes</td>
<td>16</td>
<td>2200</td>
</tr>
<tr>
<td>8088</td>
<td>8-bit</td>
<td>16 KB</td>
<td>18</td>
<td>3500</td>
</tr>
<tr>
<td>8080</td>
<td>8-bit</td>
<td>64 KB</td>
<td>40</td>
<td>6000</td>
</tr>
<tr>
<td>8085</td>
<td>8-bit</td>
<td>64 KB</td>
<td>40</td>
<td>2300</td>
</tr>
<tr>
<td>8086</td>
<td>16-bit</td>
<td>1 MB</td>
<td>40</td>
<td>29000</td>
</tr>
<tr>
<td>8088</td>
<td>8/16-bit</td>
<td>1 MB</td>
<td>40</td>
<td>29000</td>
</tr>
<tr>
<td>80186</td>
<td>16-bit</td>
<td>1 MB</td>
<td>68</td>
<td>1,200,000</td>
</tr>
<tr>
<td>80286</td>
<td>16-bit</td>
<td>16 MB real, 4 GB real</td>
<td>68</td>
<td>3,350,000</td>
</tr>
<tr>
<td>80386</td>
<td>32-bit</td>
<td>4 GB real, 64 TB virtual</td>
<td>132</td>
<td>2,750,000</td>
</tr>
<tr>
<td>80486</td>
<td>32-bit</td>
<td>4 GB real, 64 TB virtual</td>
<td>108</td>
<td>1,200,000</td>
</tr>
<tr>
<td>Pentium</td>
<td>64-bit</td>
<td>4 GB real</td>
<td>273</td>
<td>3.1 Million</td>
</tr>
<tr>
<td>Pentium Pro</td>
<td>64-bit</td>
<td>64 GB real</td>
<td>5.5 Million</td>
<td></td>
</tr>
<tr>
<td>Pentium II</td>
<td>64-bit</td>
<td>64 GB real</td>
<td>7.5 Million</td>
<td></td>
</tr>
<tr>
<td>6800</td>
<td>8-bit</td>
<td>64 KB</td>
<td>40</td>
<td></td>
</tr>
<tr>
<td>6809</td>
<td>8-bit</td>
<td>64 KB</td>
<td>40</td>
<td></td>
</tr>
<tr>
<td>68000</td>
<td>16-bit</td>
<td>16 MB</td>
<td>64</td>
<td></td>
</tr>
<tr>
<td>68020</td>
<td>32-bit</td>
<td>4 GB</td>
<td>169</td>
<td>2,000,000</td>
</tr>
<tr>
<td>68030</td>
<td>32-bit</td>
<td>4 GB</td>
<td>169</td>
<td>2,000,000</td>
</tr>
<tr>
<td>68040</td>
<td>32-bit</td>
<td>4 GB</td>
<td>169</td>
<td>2,000,000</td>
</tr>
<tr>
<td>Z-80</td>
<td>8-bit</td>
<td>64 KB</td>
<td>40</td>
<td></td>
</tr>
<tr>
<td>Z-800</td>
<td>8-bit</td>
<td>500 KB</td>
<td>40</td>
<td></td>
</tr>
<tr>
<td>Z-8000</td>
<td>16-bit</td>
<td>64 KB</td>
<td>48</td>
<td></td>
</tr>
</tbody>
</table>

---

### ACE Academy

- All IBM Personal Computers use 8088 microprocessors as CPU.
- Virtual memory concept was first introduced in 80286 microprocessors.
- 8088 microprocessor has external 8-bit data path and all internal operations are of 16-bit.
- The microprocessors primarily perform four operations: Memory Read, Memory Write, I/O Read and I/O Write. For each operation it generates the appropriate control signal.
- 8085 Microprocessor
  - It is a 40-pin IC, requires +5V single power supply.
  - Address bus width of 8085 is 16-bit. Its addressing capacity is $2^{16} = 65,536 = 64 K$ ($1 K = 1024$)
  - Low order address Bus $A_{15}, A_{14}$ is multiplexed with data bus $D_0, D_1$
  - Maximum clock frequency of 8085 microprocessor is 3.07 MHz.
  - 8085 microprocessor has on-chip clock generation facility
  - Crystal frequency of 8085 processor is 6.144 MHz. It is always double to that of clock frequency.
  - Clock frequency of 8085 is always half of the crystal frequency.
  - Theoretical value of clock frequency is 3 MHz and Crystal frequency is 6 MHz.
  - 8085 microprocessor is having 74 basic instructions with 246 opcodes.
  - It supports five hardware interrupts and eight software interrupts.
  - Hardware Interrupts: TRAP, RST 7.5, RST 6.5, RST 5.5 and INTR.
  - TRAP
    - TRAP is also called RST 4.5. TRAP is high priority interrupt and INTR is low priority interrupt.
  - Software Interrupts: RST n (RST : Restart) where n = 0 to 7
  - Length of 8085 instructions vary from one to three bytes.
  - 8085 supports five status flags: Sign (S), Zero (Z), Auxiliary Carry (Ac), Parity (P) and Carry (C).
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Introduction to Microprocessors

- ALE (Address Latch Enable) signal is used to latch low order 8-bit address present on AD0–AD7 into external latches.
- S1, S0 and IO/M signals are called status signals.
- RD and WR signals are control signals.
- HOLD and HLDA signals are used for DMA (Direct Memory Access) operation.
- READY signal is used by the microprocessor to communicate with slow operating peripherals.
- RESET IN is chip reset which is active low signal.
- RESETOUT signal is used to connect to RESET IN of other interfacing circuits used in microprocessor based system.
- CLOCKOUT of 8085 will be connected to CLOCK IN of other interfacing circuits used in micro based systems to synchronize the operation with 8085.
- 8085 uses S0 and S1 signals to indicate the current status of the processor.

\[
\begin{array}{|c|c|c|}
\hline
S_1 & S_0 & \text{Status} \\
\hline
0 & 0 & \text{Hall} \\
0 & 1 & \text{Write} \\
1 & 0 & \text{Read} \\
1 & 1 & \text{Fetch} \\
\hline
\end{array}
\]

- Getting/reading an instruction code from Memory into the processor is called opcode fetch.
- By Combining the status signal IO/M with control signals RD and WR, we can generate four different signals:

<table>
<thead>
<tr>
<th>IO/M</th>
<th>RD</th>
<th>WR</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>MEMR</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>MEMW</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>RDB</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>ROW</td>
</tr>
</tbody>
</table>

- DMA is having highest priority over all the interrupts.
- RST 7.5, RST 6.5, RST 5.5, RST 4.3 (TRAP) are called hardware vectored interrupts.

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Microprocessors

- 8085 Microprocessor consists of two 16-bit address register: Program Counter (PC) and Stack Pointer register (SP).
- PC always holds address of next memory location to be accessed.
- SP always holds address of the top of the stack.
- 8085 consists of six 8-bit general purpose registers which are accessible to the programmer: B, C, D, E, H and L.
- Based on requirement six 8-bit general purpose registers can be used as three register pairs: BC, DE and HL.
- 8085 also contains an 8-bit processor register called Accumulator 'A'.
- Range of addresses generated by 8085 Microprocessor: 0000H to FFFFH.
- The number of Machine cycles required to execute an 8085 instruction varies from one to five.

Signal description of 8085:

- All the available (40) signals of 8085 can be classified into six groups: (1) Power supply & Frequency signals (2) Serial I/O ports (3) Address Bus (4) Data Bus (5) Interrupts and externally initiated (6) Status, Control & Acknowledge signals.

SD  
SOC  
TRAP  
RST 7.5  
RST 6.5  
RST 5.5  
INTR  
HOLD  
READY  
RESET IN

8085

- Pair of signals used for Serial I/O communication: SILD & SOD
- Pair of Instructions used for Serial I/O Communication: SBTM & RDM

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> The vectored address corresponds to each of the HW vectored interrupts are given below

<table>
<thead>
<tr>
<th>Interrupt</th>
<th>Type</th>
<th>Instruction</th>
<th>Hardware</th>
<th>Trigger</th>
<th>Vector</th>
</tr>
</thead>
<tbody>
<tr>
<td>TRAP</td>
<td>Nonmask</td>
<td>Independent of EI &amp; DI</td>
<td>No external Hardware</td>
<td>Level &amp; Edge sensitive</td>
<td>0014</td>
</tr>
<tr>
<td>RST 7.5</td>
<td>Maskable</td>
<td>Controlled by EI &amp; DI Unmasked by SIM</td>
<td>No external Hardware</td>
<td>Edge sensitive</td>
<td>003C</td>
</tr>
<tr>
<td>RST 6.5</td>
<td>Maskable</td>
<td>Controlled by EI &amp; DI Unmasked by SIM</td>
<td>No external Hardware</td>
<td>Level sensitive</td>
<td>0014</td>
</tr>
<tr>
<td>RST 5.5</td>
<td>Maskable</td>
<td>Controlled by EI &amp; DI Unmasked by SIM</td>
<td>No external Hardware</td>
<td>Level sensitive</td>
<td>002C</td>
</tr>
<tr>
<td>INTR</td>
<td>Maskable</td>
<td>Controlled by EI &amp; DI</td>
<td>RST Code from external Hardware</td>
<td>Level sensitive</td>
<td>0000 To 0038</td>
</tr>
</tbody>
</table>

> INTR is a non vectored interrupt

> TRAP is a Non-Maskable Interrupt. It is always in enable condition

> RST 7.5, RST 6.5, RST 5.5, INTR are called maskable interrupts. These interrupts can be disabled by the execution of "DI" instruction can be re-enabled by the execution of "EI" instruction.

> RST 7.5, RST 6.5, RST 5.5, INTR are called Maskable Vectored interrupts

> TRAP is a non-maskable vectored interrupt

> RST 7.5, RST 6.5, RST 5.5 are called Maskable Vectored interrupts

> INTR is a maskable non vectored interrupt

> RST 7.5 is edge triggered

> RST 6.5, RST 5.5, INTR are level triggered

> TRAP is both level and edge triggered

> Vectored addresses correspond to the SW interrupts

<table>
<thead>
<tr>
<th>RST 0</th>
<th>0000 H</th>
</tr>
</thead>
<tbody>
<tr>
<td>RST 1</td>
<td>0008 H</td>
</tr>
<tr>
<td>RST 2</td>
<td>0010 H</td>
</tr>
<tr>
<td>RST 3</td>
<td>0018 H</td>
</tr>
<tr>
<td>RST 4</td>
<td>0020 H</td>
</tr>
<tr>
<td>RST 5</td>
<td>0028 H</td>
</tr>
<tr>
<td>RST 6</td>
<td>0030 H</td>
</tr>
<tr>
<td>RST 7</td>
<td>0038 H</td>
</tr>
</tbody>
</table>

> SIM instruction is used for serial output data operation as well as to mask or unmask different maskable vectored interrupts

> BIM instruction is used for serial input data operation as well as to read the status of different Maskable Vectored interrupts

> The Accumulator register (A) is also called processor register

> BORS is having 8-bit flag register which is also called status register

Flags register

The ALU includes five flip-flops that are set or reset according to data conditions in the accumulator and other registers. These flags are affected by the arithmetic and logic operations in the ALU. The flags generally reflect data conditions in the accumulator. The structure of flags register is shown below. It consists of five flags namely Sign flag (S), Zero flag (Z), Auxiliary Carry flag (Ac), Parity flag (P) and Carry flag (C).

\[ S \quad Z \quad X \quad Ac \quad P \quad X \quad C \]

**Sign flag**: In case of arithmetic operations with signed numbers, the most significant bit D7 is reserved to indicate sign information, and the remaining seven bits are used to represent the magnitude of the number. After the execution of an arithmetic or logic operation, the MSB of the result (usually in the accumulator) is copied into sign flag. S = 1 indicates result is negative, S = 0 indicates result is positive.
**Zero flag**: Z = 1 if the ALU operation results in zero. Z = 0 if the result is not zero.

**Auxiliary carry flag**: In an arithmetic operation, the carry obtained from D1 to D2 bit position is called Auxiliary carry. This flag is used only internally for BCD operation and is not available for the programmer to change the sequence of a program with a jump instruction.

**Parity flag**: After ALU operation, the result has an even number of 1's then P = 1 otherwise P = 0.

**Carry flag**: If an arithmetic operation results in a carry, the carry flag is set (i.e. CY = 1) otherwise it is reset. The carry flag also serves as a borrow flag for subtraction.

**Note**: Among the five flags, the Ac flag is used internally for BCD arithmetic; the instruction set does not include any conditional jump instructions based on this flag.

> **Accumulator register content and status register content together are called PSW (Program Status Word or processor status word)**

<table>
<thead>
<tr>
<th>A</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

> **Instruction set of 8085 Microprocessor can be classified based on their operation and length of instruction**

Classification Based on operation:

> **Data transfer instructions**: These instructions are used to transfer data from register to register, memory or from memory to register. No flags will be affected for these instructions. r1, r2, r3 may be any one out of B, C, D, E, H, L, A and r2 can be any one out of three register pairs BC, DE, HL.

<table>
<thead>
<tr>
<th>MOV, MOVM, MOV M, MOV r, MOV r, M</th>
<th>r2 ← (r1); r3 ← (r1); r1 ← (M) or (r1) ← (HL); r1 ← (M)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MVI (nM), d4, d8 = (8-bit data)</td>
<td>r ← (8-bit data)</td>
</tr>
<tr>
<td>LDI 16-bit bit address</td>
<td>r ← (H or M)</td>
</tr>
<tr>
<td>STA 16-bit address</td>
<td>r ← (HL)</td>
</tr>
<tr>
<td>LHAL 16-bit address</td>
<td>r ← (HL)</td>
</tr>
<tr>
<td>SHLD 16-bit address</td>
<td>r ← (HL)</td>
</tr>
<tr>
<td>LDAX r3</td>
<td>r ← (HL)</td>
</tr>
<tr>
<td>STAX r3</td>
<td>r ← (HL)</td>
</tr>
<tr>
<td>XCHG</td>
<td>(HL) ← (HL)</td>
</tr>
<tr>
<td>PCHL</td>
<td>(PC) ← (HL)</td>
</tr>
</tbody>
</table>

> **In 8085, the service of AC flag is used by only one instruction. It is DAA.**

> **For DAA, DCR instructions no flags affected**

> **Following table shows the list of flags affected for different instructions**

<table>
<thead>
<tr>
<th>Instruction</th>
<th>S</th>
<th>Z</th>
<th>Ac</th>
<th>P</th>
<th>Cy</th>
</tr>
</thead>
<tbody>
<tr>
<td>INI, DCR</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>DAD</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>ADD, ADC, SUB, SBB, DAA</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
</tbody>
</table>

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Logical Instructions: This group consists of AND, OR, NOT, XOR, Compare and

Rotate operations:

- ORA r (A) ← (A) V (r)
- ORA M (A) ← (A) V (M)
- ORI d8 (A) ← (A) V d8
- ANA r (A) ← (A) A (r)
- ANA M (A) ← (A) A (M)
- AND d8 (A) ← (A) A d8
- XRA r (A) ← (A) V (r)
- XRA M (A) ← (A) V (M)
- XRL d8 (A) ← (A) V d8
- CMP r (A) ← r (O)
- CMP M (A) ← M (O)
- CFI d8 (A) ← d8
- CMA (A) ← (A)
- CMC C y ← C y
- STC C y ← 1
- RLC Rotate accumulator left
- RAL Rotate Accumulator left through carry
- RRC Rotate accumulator right
-RAR Rotate Accumulator right through carry

Following table shows how flags affected for different logical instructions:

<table>
<thead>
<tr>
<th>Instruction</th>
<th>S</th>
<th>Z</th>
<th>A</th>
<th>P</th>
<th>C</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>ANA</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>ORA, XRA</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>RLC, RRC, RAL, RAR, STC, CMC</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMP, CPI</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td></td>
</tr>
</tbody>
</table>

Branch Instructions: These are also called program control transfer instructions. There are two types: Unconditional branch and Conditional branch instructions.

- No flags will be affected for branch instructions

Unconditional branch instructions:

- JMP 16 - bit address
- CALL 16 - bit address
- RET
- RST n (n = 0 to 7)

PCHL is one-byte equivalent of three byte JMP instruction
RST n is one-byte equivalent of three byte CALL instruction

Conditional branch instruction:

<table>
<thead>
<tr>
<th>Jump Instructions</th>
<th>Call Instructions</th>
<th>Return Instruction</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>J Z, 16 - bit addr</td>
<td>CZ, 16 - bit addr</td>
<td>RZ</td>
<td>IF Z = 1</td>
</tr>
<tr>
<td>JNZ, 16 - bit addr</td>
<td>CNZ, 16 - bit addr</td>
<td>RNZ</td>
<td>IF Z = 0</td>
</tr>
<tr>
<td>JC 16 - bit addr</td>
<td>CC, 16 - bit addr</td>
<td>R C</td>
<td>IF Cy = 1</td>
</tr>
<tr>
<td>JNC, 16 - bit addr</td>
<td>CNC, 16 - bit addr</td>
<td>RNC</td>
<td>IF Cy = 0</td>
</tr>
<tr>
<td>JP 16 - bit addr</td>
<td>CP, 16 - bit addr</td>
<td>RP</td>
<td>IF S = 1</td>
</tr>
<tr>
<td>JNC, 16 - bit addr</td>
<td>CM, 16 - bit addr</td>
<td>RM</td>
<td>IF S = 0</td>
</tr>
<tr>
<td>JPO, 16 - bit addr</td>
<td>CPO, 16 - bit addr</td>
<td>RPO</td>
<td>IF F = 0</td>
</tr>
<tr>
<td>JPE, 16 - bit addr</td>
<td>CPE, 16 - bit addr</td>
<td>RPE</td>
<td>IF F = 1</td>
</tr>
</tbody>
</table>

Machine Control, Stack and IO related Instructions: No flags affected for these instructions.

- Machine Control: EI, DI, SIM, RIM, NOP, HLT
- Stack related: PUSH r (r = BC, DE, HL)
- POP r
- POP PSW
- LXI SP, 16 - bit addr
- SPHL

IO Related:

IN 8 - bit Port address
OUT 8 - bit Port address

Classification of Instructions as per their length:

- According to the length of instruction, the 8085 instructions can be classified into three groups:

1. One byte or One-word instructions: This type of instruction requires one memory location to store in memory. The one byte instructions include both Op code and Operand in the same byte. E.g. MOV A, C, ADD B, CMA etc.

2. Two byte or Two-word instructions: This type of instruction requires two memory locations to store in memory. In a two byte instruction, the first byte specifies the operation code and the second byte specifies the operand. E.g. MOV A, 44 H, ADI 36 H, SUI 78 H, ORI 167 H, XRI 9A H etc.
3. Three byte or Three-word instructions: This type of instruction requires three memory locations to store in the memory. In three byte instruction, the first byte specifies the op code, and the following two bytes specify the 16-bit address or data.
   E.g: JMP 2500 H, STA 4509 H, LDA 3456 H, LXH 2345 H etc.

One byte instructions can be recognized as follows:

a) Data transfer instructions that copy the contents from one register (or memory) into another register (or memory) are one-byte instructions. E.g: MOV

b) Arithmetic/logic instructions without the ending letter 'T' are one byte.
   E.g: ADD, SUB, ORA

Two byte instructions can be recognized as follows:

a) Instructions that load or manipulate 8-bit data directly are 2-byte instructions.
   E.g: MVI, ADI, SUI, SBI, IN, OUT, ORI, XRI, ANI etc.

b) All three letter instructions with ending letter 'T' (except LXI) are two byte instructions.

- The instructions that load 16 bits or refer to memory addresses are 3-byte instructions.
  E.g: LXO, JMP, Conditional Jumps, CALL, Conditional Calls, STA, LDA, LHLD, SHLD.

- Whenever PUSH instruction is executed, SP register content is decremented by 2.

- Whenever POP instruction is executed, SP register content is incremented by 2.

- When CALL instruction (conditional or unconditional) or RST instruction is executed, SP register content is decremented by 2, because current context of PC will be pushed automatically on to top two locations of the stack.

- When RET instruction (Conditional or Unconditional) is executed, SP register content is incremented by 2, because top two locations of the stack are retrieved and loaded into PC

---

<table>
<thead>
<tr>
<th><strong>ACE Academy</strong></th>
<th><strong>Introduction to Microprocessors</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>3. Three byte or Three-word instructions:</strong> This type of instruction requires three memory locations to store in the memory. In three byte instruction, the first byte specifies the op code, and the following two bytes specify the 16-bit address or data.</td>
<td></td>
</tr>
<tr>
<td>E.g: JMP 2500 H, STA 4509 H, LDA 3456 H, LXH 2345 H etc.</td>
<td></td>
</tr>
</tbody>
</table>

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- The instructions that load 16 bits or refer to memory addresses are 3-byte instructions. E.g: LXO, JMP, Conditional Jumps, CALL, Conditional Calls, STA, LDA, LHLD, SHLD.

---

<table>
<thead>
<tr>
<th><strong>COMPARISON OF PUSH AND POP INSTRUCTIONS WITH CALL AND RET INSTRUCTIONS</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>PUSH and POP</strong></td>
</tr>
<tr>
<td>The programmer uses the instructions PUSH to save the contents of register Specified register pair on the stack.</td>
</tr>
<tr>
<td>When PUSH is executed, the stack pointer register is decremented by two.</td>
</tr>
<tr>
<td>The instruction POP transfers the contents of the top two locations of the stack to the specified register pair.</td>
</tr>
<tr>
<td>When the instruction POP is executed, the stack pointer is incremented by two.</td>
</tr>
<tr>
<td>There are no conditional PUSH and POP instructions.</td>
</tr>
</tbody>
</table>

---

<table>
<thead>
<tr>
<th><strong>Addressing Modes:</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>The way in which the operand information is specified in the instruction code is called addressing mode. The 8085 microprocessor supports five addressing modes.</td>
</tr>
</tbody>
</table>

1. **Implied or Implicit or Inherent addressing mode:** There are certain instructions which operate on the content of the accumulator. Such instructions do not require the address of the operand. E.g: CMA, STC, RLC, RRC, RAL, RAR etc.

2. **Direct addressing mode:** In this mode the address of the operand (data) is given in the instruction itself. E.g: STA, LDA, SHLD, LHLD, IN, OUT etc.

3. **Register addressing mode:** In this mode the operands are in the general purpose registers. The operation code specifies the address of the register in addition to the operand to be performed. E.g: MOV A, B; ADD A, B; SUB C; ORA A; B etc.

4. **Register Indirect addressing mode:** In this mode the address of the operand is specified by a register pair. E.g: LXI, LDX, LDA etc.

5. **Immediate addressing mode:** In this mode the operand is specified in the instruction itself. E.g: MVI, ADI, LXI, ORI, SUI, SBI, ACI, XRI, ANI etc.

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Each instruction cycle of the 8085 microprocessor can be divided into a few basic operations called machine cycles, and each machine cycle can be divided into T-states.

Machine cycle: It is defined as the time required to complete the operation of accessing either memory or I/O. In the 8085, the machine cycle may consist of three to six T-states.

T-state is defined as one sub-division of the operation performed in one clock-period.

The time required to complete the execution of an instruction is called instruction cycle.

The 8085 instruction cycle consists of one to five machine cycles or one to five operations.

The first machine cycle of 8085 consists of four to six T-states and all other subsequent machine cycles consist of four T-states only.

Read or write signal is generated at the beginning of T2 and will be completed before the end of T3 in every machine cycle.

Types of machine cycles of 8085: Op Code fetch cycle, Memory read cycle, Memory write cycle, I/O read cycle, I/O write cycle, interrupt acknowledge machine cycle and bus idle machine cycle.

The first machine cycle of each instruction cycle is always Opcode fetch cycle.

In 8085, CALL instruction is the lengthy instruction which takes 18-T states and the shortest instruction takes only 4 T-states (Eg: MOV A, B).

First machine cycle with four T-states is essential for each and every instruction. Other machine cycles depend on operation of the instruction.

ALE signal is generated during T1 state of each machine cycle.

Machine cycle format is given below:

<table>
<thead>
<tr>
<th>M1</th>
<th>M2</th>
<th>M3</th>
<th>M4</th>
<th>M5</th>
</tr>
</thead>
<tbody>
<tr>
<td>T1</td>
<td>T2</td>
<td>T3</td>
<td>T4</td>
<td>T5</td>
</tr>
</tbody>
</table>

| Mapping: Assigning addresses to I/O devices or memory locations is called mapping.
| Memory mapping: Assigning address to memory locations is called memory mapping.
| Memory mapping can be changed by changing the hardware logic used for the chip selection.
| To interface a memory chip with the 8085, the necessary low-order address lines of the 8085 address bus are connected to the address lines of the memory chip. The high-order address lines are decoded to generate CS (chip select) signal to enable the chip.

I/O devices can be connected to microprocessor in two different techniques:

1. Memory mapped I/O technique
2. I/O mapped or Peripheral mapped I/O technique

Memory mapped I/O technique:

- In memory mapped I/O, the I/O devices are also treated as memory locations, under that assumption they will be given 16-bit address.
- In memory mapped I/O, microprocessor uses memory related instructions to communicate with I/O devices. E.g: STA, LDA, MOV A,M; MOV M,A etc.
- In memory mapped I/O, MEMR and MEMW control signals are used to activate I/O devices.
- In memory mapped I/O, one entire memory map is shared by memory locations and I/O devices. One address can be used only once. This technique is used in a system where the number of I/O devices are less.

The maximum numbers of I/O devices that can be connected to microprocessor in this technique are 65536.

I/O mapped I/O technique:

- In this technique the I/O devices are identified by the microprocessor with separate 8-bit port address.
- This technique uses separate control signals (OE and R/W) to activate I/O devices and separate instructions (IN and OUT) to communicate with I/O devices.
- In this technique I/O mapping is independent of memory mapping. Same address can be used to identify input device and output device.

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Interfacing: Designing hardware circuit and writing software instructions to enable the microprocessor to communicate with peripheral devices is called interfacing. And the hardware circuit is called the interfacing device.

- There are two basic types of interfacing devices are available.
  1. Non-programmable interfacing devices and
  2. Programmable interfacing devices.

Non-programmable interfacing devices: Once the microprocessor based system is designed it is not possible to program this type of devices. Examples: 8212: Non-programmable I/O port, 74L245; bi-directional buffers, 74L573 - transparent latches etc.

Programmable interfacing devices: Writing a specific word, called the control word, according to the internal logic, can program a programmable interfacing device.

1. 8155 - Programmable Peripheral Interface (PPI) device with 256 bytes RAM and 16-bit timer/counter. It is a general purpose interfacing device i.e. it can be used to interface variety of I/O devices to the microprocessor.
2. 8255 - PPI It is also called programmable interface adapter (PIA). It consists of three 8-bit ports.
3. 8253 - Programmable Interval Timer. It can work in six different modes:
   - Mode 0 - Interrupt on terminal count
   - Mode 1 - Programmable one shot
   - Mode 2 - Free generator
   - Mode 3 - Square wave generator
   - Mode 4 - Software Triggered strobe
   - Mode 5 - Hardware Triggered strobe
4. 8251 - Programmable communication interfacing device. It is also called USART (Universal Synchronous Asynchronous receiver transmitter).
5. 8257 - Programmable DMA (Direct Memory Access) controller, DMA transfer is an I/O technique used commonly for high speed data transfer. The 8257 is a four channel DMA controller.
1. Which of the following microprocessors is not an 8-bit microprocessor?
   (a) 8085  (b) Z-80  (c) 68000  (d) 6502

2. Which of the following microprocessor has a 16-bit data bus?
   (a) 8085  (b) Z-80  (c) 68000  (d) 6502

3. A microprocessor consists of
   (a) a microprocessor  (b) memory  (c) I/O devices  (d) all of the above

4. Which of the following statements is false?
   (a) A processor has a bi-directional address bus
   (b) A microprocessor has an 8-bit address bus
   (c) A microprocessor has a 16-bit data bus
   (d) A microprocessor has an ALU

5. The address bus of an 8-bit microprocessor is
   (a) Unidirectional  (b) bidirectional
   (c) Either unidirectional or bidirectional  (d) None

6. The data bus of an 8-bit microprocessor is
   (a) Unidirectional  (b) bi-directional
   (c) Either unidirectional or bidirectional  (d) None

7. The data bus of an 8-bit microprocessor is
   (a) Unidirectional  (b) bi-directional
   (c) Either unidirectional or bi-directional  (d) None

8. Which of the following microprocessors is used in
   (a) 8085  (b) 8-bit  (c) 16-bit  (d) 20-bit

9. The word size of 8085 microprocessor is
   (a) 8-bit  (b) 6-bit  (c) 8-bit  (d) 20-bit

10. Which of the following microprocessors have
    (a) 8-bit  (b) 16-bit  (c) 20-bit  (d) None

11. The address bus width of a microprocessor which is capable of
    (a) 8  (b) 16  (c) 64K  (d) 256K

12. Which of the following microprocessors are capable of
    (a) 8-bit  (b) 16-bit  (c) 32-bit  (d) 64-bit

13. Which of the following microprocessors can have
    (a) 8-bit  (b) 16-bit  (c) 32-bit  (d) None

14. A microprocessor has an 8-bit Op Code. The maximum possible
    number of Op Codes for this microprocessor will be
    (a) 256  (b) 64  (c) 8  (d) 16

15. The Program Counter in a microprocessor always holds
    (a) the number of programs being executed by the microprocessor
    (b) the number of instructions being executed on the microprocessor
    (c) the number of interrupts handled by the microprocessor
    (d) the address of the next instruction to be fetched.

16. The stack pointer register in a microprocessor
    (a) contains the number of programs being executed on the microprocessor
    (b) contains the number of instructions being executed on the microprocessor
    (c) holds the address of the next instruction to be fetched
    (d) holds the address of the top of the stack.

17. Which of the following statements is false?
    (a) A microprocessor has a bidirectional address bus
    (b) A microprocessor has a unidirectional address bus
    (c) A microprocessor has a bidirectional data bus
    (d) A microprocessor has an ALU

18. Which of the following microprocessors are present in the 8085
    microprocessor?
    (a) 8-bit  (b) 16-bit  (c) 6-bit  (d) 20-bit

19. Which of the following microprocessors are present in the 8085
    microprocessor?
    (a) 8-bit  (b) 16-bit  (c) 32-bit  (d) None

20. The number of status flags present in 8085 microprocessor are
    (a) 6  (b) 5  (c) 4  (d) 3

21. The number of hardware interrupts present in 8085 microprocessor are
    (a) 5  (b) 4  (c) 3  (d) 2

22. Which of the following statements is false?
    (a) A microprocessor has a bidirectional address bus
    (b) A microprocessor has a unidirectional address bus
    (c) A microprocessor has a bidirectional data bus
    (d) A microprocessor has an ALU

23. Identify the non-stackable interrupt from the following
    (a) RST 7.5  (b) RST 6.5  (c) RST 5.5  (d) RST 4.5

24. In microprocessor based systems DMA refers to
    (a) direct memory access for the microprocessor
    (b) direct memory access for the user
    (c) direct memory access for the I/O device
    (d) None of the above

25. What is the interrupt facility provided in a microprocessor?
    (a) change the sequence of instructions being executed
    (b) stop the microprocessor when desired
    (c) stop the microprocessor when signals from I/O devices are received
    (d) keep a count on the working of the microprocessor

26. In a microprocessor, what is the function of the programs
    (a) 8-bit  (b) 16-bit  (c) 32-bit  (d) None

27. Which of the following microprocessors are present in the 8085
    microprocessor?
    (a) 8-bit  (b) 16-bit  (c) 6-bit  (d) 20-bit

28. Which of the following microprocessors are present in the 8085
    microprocessor?
    (a) 8-bit  (b) 16-bit  (c) 32-bit  (d) None

29. Which of the following microprocessors are present in the 8085
    microprocessor?
    (a) 8-bit  (b) 16-bit  (c) 6-bit  (d) 20-bit

30. Which of the following microprocessors are present in the 8085
    microprocessor?
    (a) 8-bit  (b) 16-bit  (c) 32-bit  (d) None
26. A microprocessor differentiates between op-codes, data/address at any time by
   (a) the sequence in which memory contents are fetched
   (b) its internal registers
   (c) the stack pointer
   (d) the program counter

27. A microprocessor without the interrupt facility
   (a) is best suited for a process control system
   (b) is not useful for a process control system
   (c) can not be used for DMA operation
   (d) can not be interfaced with any I/O device

28. In microprocessor based systems I/O ports are used to interface
   (a) The I/O devices and memory
   (b) the IP-device only
   (c) The OP-devices only
   (d) all the I/O devices

29. The stack pointer
   (a) Resides in RAM
   (b) resides in microprocessor
   (c) Resides in ROM
   (d) may be in RAM or ROM

30. In a microprocessor based system, the stack is always in
   (a) Microprocessor
   (b) RAM
   (c) ROM
   (d) EPROM

31. The instruction set of a microprocessor
   (a) is specified by the manufacturer
   (b) is specified by the user
   (c) Can not be changed by the user
   (d) is stored inside the microprocessor

32. An 8085 microprocessor uses a crystal of frequency 6.25 MHz.
    The 7 state value is
   (a) 340ns   (b) 640ns
   (c) 960ns   (d) 1280ns

33. In an 8085 microprocessor based system, the contents of SP is
    1000H. PUSH B instruction will transfer the contents of
    registers B and C respectively for memory locations
   (a) 0FFH and 0FFFH
   (b) 0FFH and 00FFH
   (c) 000H and 00FFH
   (d) 1000H and 1001H

34. In an 8085 microprocessor based system, the contents of
    SP are 2000H. POP H instruction will transfer the contents
    of memory location
    (a) 2001H and 2002H to H and L registers respectively
    (b) 2001H and 2000H to H and L registers respectively
    (c) 2000H and 1FFFH to H and L registers respectively
    (d) 2000H and 1999H to H and L registers respectively

35. PUSH H instruction in 8085 microprocessor causes
    (a) the contents of register B only to be copied in the stack
    (b) the contents of register B and C to be copied in the stack
    (c) the contents of registers B and C to be transferred in the stack
    (d) the registers get cleared

36. SUB A instruction in 8085
    (A) resets carry and sign flags
    (B) resets zero and parity flags
    (C) sets zero and sign flags
    (D) sets zero and carry flags

37. In 8085 microprocessor, the accumulator contains the value 0A3H
    and register C contains the value 05H. After CMPC instruction is
    executed the
    (a) zero and carry flags will be set
    (b) zero and carry flags will be reset
    (c) zero flag will be set and the carry flag will be reset
    (d) zero flag will be reset and the carry flag will be set

38. When an 8085 microprocessor is reset, the address bus contains
    (a) 0000H   (b) 002CH
    (c) 0043H   (d) 005CH

39. Which of the data transfer is not possible in microprocessor
    (a) memory to accumulator
    (b) accumulator to memory
    (c) memory to memory
    (d) I/O device to accumulator

40. In 8085 microprocessor, in response to BST 7.5 instructions, the execution is
    transferred to memory location
    (a) 0000H   (b) 002CH
    (c) 0043H   (d) 005CH

41. In 8085 microprocessor, which of the following statements is false?
    (a) there is a pin available for serial input
    (b) there is a pin available for serial output
    (c) serial I/O is possible through EIM and EIM instructions
    (d) serial I/O is not possible

42. EPROM are preferred for storing programs while developing new
    microprocessor based system because of their
    (a) non-volatile characteristic
    (b) erasable and programmable characteristic
    (c) random access characteristic
    (d) all the above characteristics
47. cycle-sealing mode of DMA operation involves
(a) DMA controller taking over the address, data, and control paths while a block of data is transferred between memory and I/O devices.
(b) During the read or write operation, the DMA controller takes over and manages the transfer of data between memory and I/O devices.
(c) Data transfer takes place between the I/O device and memory during alternate count cycles.
(d) The DMA controller waits for the interrupt from the microprocessor to finish the execution of the program and then takes over the bus.

50. Which of the following interrupt is both level and edge sensitive?
(a) NMI
(b) INTR
(c) TRAP
(d) Neither

51. The addressing mode used in the instruction PUSH B is
(a) direct
(b) register
(c) indirect
(d) immediate

52. On receiving an interrupt from an I/O device, the CPU
(a) halts for a predetermined time
(b) halts over control of address bus and data bus to the interrupting device
(c) branches off to the interrupt service routine immediately
(d) branches off to the interrupt service routine after completion of the current instruction.

53. The ALE line of an 8085 microprocessor is used to
- broadcast the output of an I/O location into an external bus
- debounce the open-collector signals from memory devices
- latch the 8-bit data line AD7-AD0 into an external latch
- indicate the status of the TRAP interrupt

54. What is the execution time for the instruction, "STAADD0", in an 8085 microprocessor if the clock frequency is 3 MHz?
(a) 429ns
(b) 397ns
(c) 311ns
(d) 369ns

55. The following instruction needs two clocks for execution because of the two clocks for microcycles.
(a) SUBA
(b) XRA
(c) OVA
(d) MVC

56. Which of the following is true if ALU is in carry mode?
(a) NMI
(b) INTR
(c) TRAP
(d) Neither

57. The 8085 microprocessor will enter INTA state after the recognition of
(a) NMI
(b) TRAP
(c) INTR
(d) Neither

58. Which of the following files the interrupts in decreasing priority?
(a) TRAP, NMI, INTA, INTB
(b) INTB, NMI, INTA
(c) INTA, NMI, INTB
(d) NMI, INTA, INTB

59. Which of the following is the upper limit for the interrupt vector address for
(a) TRAP
(b) INTR
(c) TRAP, NMI
(d) Neither
GATE Examination Questions

Electronics & Communication Engineering

Q1. In a microprocessor, the service routine for a certain interrupt starts from a fixed location in memory which cannot be externally set, but the interrupt can be delayed or rejected. Such an interrupt is
(a) non-maskable and non- vectored
(b) maskable and non-vectored
(c) non-maskable and vectored
(d) maskable and vectored

GATE-2008 (ECE)

Q2. An 8085 executes the following instructions:

GATE-2009 (ECE)

Q3. An 8255 chip is interfaced to an 8085 microprocessor system as an I/O mapped I/O as shown in the figure. The address lines A0 and A1 of the 8255 I/O ports are used by 8051 chip to decode internally its three ports and Control register. The address lines A3 to A7 as well as the signal are used for address decoding. The range of addresses for which the 8255 chip would get selected is

GATE-2009 (ECE) - 2 marks each

GATE-2007 (ECE)
GATE Examination Questions

114

Statements for linked questions Q4 and Q5

An 8085 assembly language program is given below

Line 1: MOV A, 00H
2: MOV B, 0E H
3: XRI 00H
4: ADD B
5: ANL AB H
6: CPI BF H
7: STA 3010H
8: HLT

Q4. The content of the accumulator just after execution of the ADC instruction in line 4 will be
(a) CF = 1 (b) EA = 1 (c) DC = 1 (d) DF = 1

Q5. After execution of line 7 of the program, the status of the CY and Z flags will be
(a) CY = 0, Z = 0 (b) CY = 0, Z = 1 (c) CY = 1, Z < 0 (d) CY = 1, Z = 1

GATE - 2006 (ECE) - 2 marks each

Q6. An I/O Peripheral device shown in figure (a) is interfaced to an 8085 microprocessor. To select the I/O device in the I/O address range D4 H to D7 H. The chip-select (CS) should be connected to the output of the decoder shown in figure (a) below.

Q7. Following is the segment of an 8085 assembly language program

LXI SP, 00FFH
CALL 3000H
3000: LDI, 3CF4H
PUSH PSW
POP PSW
PUSH FL
RET

On completion of JBP execution, the contents of SP is
(a) 3CF8H (b) 3CF4H (c) 3FFD H (d) 3FFF H

Notes:

ACE Academy

Microprocessors

115

GATE - 2005 (ECE) - 2 marks each

Q6. What memory address range is NOT represented by Chip 1 and Chip 2 in the figure A1-A15? In this figure are address less and CS means chip select.

A1 - A7

15 bytes

Chip 1

A8

A9

A10

A11 - A15

256 bytes

Chip 2

(a) 0100 - 02FF H (b) 1500 - 16FF H
(c) F900 - FAFF H (d) F800 - FIFF H

Statements for linked questions Q6 and Q6.

Consider an 8085 microprocessor system

Q6. The following program starts at 0100 H

LXI SP, 00FFH
LXI H, 0107H
MVI A, 30H
ADI M

The contents of accumulator when the program counter
frees up 0109H is
(a) 20H (b) 02H (c) 00H (d) FFH

Q10. If in addition following code flows from 010B H onwards.

CHI 40H
ADD M

What will be the result in the accumulator after the last instruction is executed?
(a) 40H (b) 20H (c) 60H (d) 42H

Notes:

ACE Academy
Q14. The 8255 Programmable Port Interfacing is used as described below:
(i) An A/D converter is interfaced to a microprocessor through an 8255. The conversion is initiated by a signal from the 8255 on Port C. A signal on Port C causes data to be shifted into Port A.
(ii) Two computer exchange data using a pair of tristate Port A works as a bidirectional port supported by appropriate handshaking signals.

The appropriate modes of operation of the 8255 for (i) and (ii) would be
(a) Mode 1 for (i) and Mode 1 for (ii)
(b) Mode 1 for (i) and Mode 2 for (ii)
(c) Mode 1 for (i) and Mode 0 for (ii)
(d) Mode 2 for (i) and Mode 2 for (ii)
(e) Mode 2 for (i) and Mode 1 for (ii)

Q15. The number of memory cycles required to execute the following 8085 instructions
(i) LOD 10000H
(ii) LDX D, P@H1 would be
(a) 1 for (i) and 2 for (ii)
(b) 3 for (i) and 3 for (ii)
(c) 3 for (i) and 3 for (ii)
(d) 4 for (i) and 3 for (ii)
(e) 3 for (i) and 4 for (ii)

Q16. Consider the sequence of 8085 instructions given below:

LDX H, 2056 H
MOV A, M
MOV M, A

Which one of the following is performed by the sequence?
(a) Contents of location 2058 are loaded to the accumulator.
(b) Contents of the location 2056 are compared with the contents of the accumulator.
(c) Contents of location 2056 are computerized and stored in accumulator.
(d) Contents of location 2052 are computerized and stored in location 5092.

Q17. It is desired to multiply the numbers 10A, H by 03 H and store the result in the accumulator. The numbers are available in registers B and C respectively. The part of the 8085 program for this purpose is given below:

MV A, 03 H
Loop:
ADD B
JNZ Loop

The sequence of instructions to complete the program would be
(a) INC, Loop
(b) ADD B
(c) DCR C
(d) JNZ Loop

Q18. An 8085 microprocessor operating at 5 MHz clock frequency executes the following routine:

START: MOV A, B
OUT 56 H
DCR B
STA FF00 H
JMP WAIT

(a) Determine the total number of machine cycles required to execute the routine till the JMP instruction is executed for the first time.
(b) Determine the time interval between two consecutive WAIT signals.
(c) If the external logic controls the READY line so that three WAIT states are inserted in the I/O WRITE machine cycle, determine the time interval between two consecutive WAIT signals.

GATE: 2003 (CECE) – 2 marks each
GATE: 2002 (CECE) – 2 marks each

Notes:

(a) Carry Flag will be set and Zero Flag will be reset.
(b) Carry Flag will be set but Zero Flag will be set.
(c) Both Carry Flag and Zero Flag will be reset.
(d) Both Carry Flag and Zero Flag will be set.

GATE: 2003 (CECE) – 2 marks each

(a) XYZ
(b) MN
(c) Abc
(d) Def

Start:

MOV A, B
OUT 56 H
DCR B
STA FF00 H
JMP WAIT

Notes:

(a) Carry Flag will be set and Zero Flag will be reset.
(b) Carry Flag will be set but Zero Flag will be set.
(c) Both Carry Flag and Zero Flag will be reset.
(d) Both Carry Flag and Zero Flag will be set.

GATE: 2003 (CECE) – 2 marks each

(a) XYZ
(b) MN
(c) Abc
(d) Def

Start:

MOV A, B
OUT 56 H
DCR B
STA FF00 H
JMP WAIT

Notes:

(a) Carry Flag will be set and Zero Flag will be reset.
(b) Carry Flag will be set but Zero Flag will be set.
(c) Both Carry Flag and Zero Flag will be reset.
(d) Both Carry Flag and Zero Flag will be set.
Q18. An 8085 microprocessor based system uses a 4K x 8 bit RAM whose starting address is A0000 H. The address of the last byte in this RAM is — 1 mark
(a) $00FF$ H  (b) $1000$ H  (c) $20FF$ H  (d) $B000$ H

Q19. Consider the following sequence of instructions for an 8085 microprocessor based system — 9 marks

<table>
<thead>
<tr>
<th>Memory Address</th>
<th>Instructions</th>
</tr>
</thead>
<tbody>
<tr>
<td>FF00</td>
<td>MVI A, FF H</td>
</tr>
<tr>
<td>FF02</td>
<td>INC A</td>
</tr>
<tr>
<td>FF03</td>
<td>JC FF0C H</td>
</tr>
<tr>
<td>FF06</td>
<td>ORI A8 H</td>
</tr>
<tr>
<td>FF08</td>
<td>JMI FF16 H</td>
</tr>
<tr>
<td>FF0B</td>
<td>XRA A</td>
</tr>
<tr>
<td>FF0C</td>
<td>OUT PORT1</td>
</tr>
<tr>
<td>FF0E</td>
<td>HLT</td>
</tr>
<tr>
<td>FF10</td>
<td>XRI FF H</td>
</tr>
<tr>
<td>FF12</td>
<td>OUT PORT2</td>
</tr>
<tr>
<td>FF14</td>
<td>HLT</td>
</tr>
<tr>
<td>FF16</td>
<td>MVI A, FF H</td>
</tr>
<tr>
<td>FF17</td>
<td>AND 02 H</td>
</tr>
<tr>
<td>FF19</td>
<td>RAL</td>
</tr>
<tr>
<td>FF1A</td>
<td>JS FF23 H</td>
</tr>
<tr>
<td>FF1D</td>
<td>JC FF10 H</td>
</tr>
<tr>
<td>FF20</td>
<td>JNC FF12 H</td>
</tr>
<tr>
<td>FF23</td>
<td>OM R</td>
</tr>
<tr>
<td>FF24</td>
<td>OUT PORT3</td>
</tr>
<tr>
<td>FF26</td>
<td>HLT</td>
</tr>
</tbody>
</table>

(a) If the program execution begins at the location FF00 H, write down the sequence of instructions which are actually executed till a HLT instruction. (Assume all flags are initially reset)
(b) Which of the three ports will be loaded with data, and what is the bit pattern of the data?

Q20. a) The program and machine code for an 8085 microprocessor are given by

<table>
<thead>
<tr>
<th>3E</th>
<th>MVI A, C3</th>
</tr>
</thead>
<tbody>
<tr>
<td>C3</td>
<td>NOP</td>
</tr>
<tr>
<td>80</td>
<td>ADD B</td>
</tr>
<tr>
<td>3D</td>
<td>DCR A</td>
</tr>
<tr>
<td>C2</td>
<td>JNZ 800A</td>
</tr>
<tr>
<td>0A</td>
<td>JMP 800C</td>
</tr>
<tr>
<td>8C</td>
<td>DC OUT 10</td>
</tr>
<tr>
<td>8D</td>
<td>76 HLT</td>
</tr>
</tbody>
</table>

The starting address of the above program is 7FFH H. What would happen if it is executed from 800H H?

S V Rao

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Q25. An instruction used to set the carry flag in a computer can be classified as
(a) data transfer
(b) arithmetic
(c) logical
(d) program control

GATE - 1987 (ECE)

Q26. In an 8085 µP system, the RST instruction will cause an interrupt
(a) only if an interrupt service routine is not being executed
(b) only if a bit in the interrupt mask is made 0
(c) only if interrupts have been enabled by an EI instruction
(d) None of the above

GATE - 1987 (ECE)

Q27. The following instructions have been executed by an 8051 µP

ADDRESS INSTRUCTION
6010 LCI H, &A 70 H
6012 MOV A, L
6014 ADD H
6015 DAA
6016 MOV H, A
6017 PCHL

From which address will the next instruction be fetched?
(a) 6019
(b) 6379
(c) 6779
(d) None of the above

Q28. An 8085 microprocessor uses a 2 MHz crystal. Find the time taken by it to execute the following delay subroutine, inclusive of the call instruction in the calling program.

Calling Program:

```
CALL DELAY
```

```
DELAY: PUSH PSW
MOV A, 68H
LOOP: NOP
DEC A
JNZ LOOP
POP PSW
RET
```

You are given that a CALL instruction takes 18 cycles of the system clock, PUSH PSW requires 12 cycles and a conditional jump takes 10 cycles if the jump is taken and 7 cycles if it is not. All other instructions used above take 1 (one) clock cycle, where n is the number of accesses to the memory, inclusive of the opcode fetch. — 5 marks

GATE - 1994 (ECE)

Q29. The following sequence of instructions is executed by an 8085 microprocessor:
1000 LXI SP, 27 FF
1003 CALL 50 H
1000 SP = 27 FF, HL = 1001
1003 POP H
The contents of the stack pointer (SP) and the HL register pair on completion of execution of these instructions are
(a) SP = 27 FF, HL = 1003
(b) SP = 27 FF, HL = 1001
(c) SP = 27 FF, HL = 1000
(d) SP = 27 FF, HL = 1001.

GATE - 1995 (ECE) – 1 mark each

Q30. When a CPU is interrupted, it
(a) stops execution of instructions
(b) acknowledges interrupt and branches to subroutine
(c) acknowledges interrupt and continues
(d) acknowledges interrupt and waits for the next instruction from the interrupting device.

GATE - 1994 (ECE)

Q31. A DMA transfer implies
(a) direct transfer of data between memory and accumulator
(b) direct transfer of data between memory and I/O devices
(c) transfer of data exclusively within the microprocessor
(d) transfer of data between memory and I/O devices.

GATE - 1996 (ECE)

Q32. An "Assembler" for a microprocessor is used for
(a) assembly of processors in a production line
(b) translation of source programs using different modules
(c) translation of a program from assembly language to a machine language
(d) translation of a higher level language into English text.

GATE - 1995 (ECE) – 1 mark each

Q33. In a microprocessor, the address of the next instruction to be executed is stored in
(a) stack pointer
(b) address latch
(c) Program counter
(d) general purpose register

GATE - 1996 (ECE)

Key:
01. d 02. c 03. a 04. b 05. a 06. c 07. d 08. c 09. b 10. a 11. b 12. c 13. c 14. a 15. b 16. c 17. 18. b 19. 20. b 21. 22. 23. 24. 25. a 26. 27. 28. 29. 30. b 31. b 32. c

GATE - 1997 (ECE) – 1 mark each

GATE - 1998 (ECE)

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**GATE: 2009 (EE)**

Q05. In an 8038 microprocessor, the contents of the Accumulator, after the following instructions are executed, will become:
- (a) 01 H
- (b) 3F H
- (c) 1F H
- (d) 10 H

**GATE: 2006 (EE)**

Q02. An input device is interfaced with Intel 8085 microprocessor using a memory mapped I/O. The address of the device is 200H. In order to input data from the device to accumulator, the sequence of instructions will be:
- (a) MOV A, 200H
- (b) MOV 200H, A
- (c) MOV A, 200H
- (d) MOV 200H, A

Q03. The contents (in Hexadecimal) of some of the memory locations in an 8085 based system is given below.

<table>
<thead>
<tr>
<th>Address</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>26FF</td>
<td>02</td>
</tr>
<tr>
<td>26FF</td>
<td>03</td>
</tr>
<tr>
<td>2700</td>
<td>00</td>
</tr>
<tr>
<td>2701</td>
<td>02</td>
</tr>
<tr>
<td>2702</td>
<td>04</td>
</tr>
</tbody>
</table>

The contents of stack pointer (SP), program counter (PC) and (P, L) are 2700H, 2100 H and 0000H respectively. Choose the following sequence of instructions are executed.
- (a) 2100H: DAV SP
- (b) 2100H: PC
- (c) the contents of (SP) and (PC) at the end of execution will be:
  - (i) (SP)=0102H, (PC)=2700H
  - (ii) (SP)=2100H, (PC)=2700H
- (d) Both SP and PC are 2100H
- (e) Both SP and PC are 2700H

Q04. Which one of the following statements regarding the INT (interrupt) and the BRQ (bus request) pins is in a CPU is correct?
- (a) The BRQ pin is sampled after every instruction cycle, but the INT pin is sampled after every machine cycle
- (b) Both INT and BRQ are sampled after every machine cycle
- (c) The INT pin is sampled after every instruction cycle, but the BRQ pin is sampled after every machine cycle
- (d) Both INT and BRQ are sampled after every instruction cycle

Q05. A software delay subroutine is written as given below:

<table>
<thead>
<tr>
<th>Label</th>
<th>Instruction</th>
</tr>
</thead>
<tbody>
<tr>
<td>DELAY</td>
<td>MOV A, 7H</td>
</tr>
<tr>
<td></td>
<td>ADD A, 00H</td>
</tr>
<tr>
<td></td>
<td>DJNZ DELAY</td>
</tr>
<tr>
<td></td>
<td>RET</td>
</tr>
</tbody>
</table>

**GATE: 2004 (EE)**

Q06. If the following program is executed in a microprocessor, the number of instruction cycles it will take from START to HALT is

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>START</td>
<td>MVA, 1H</td>
</tr>
<tr>
<td>SHIFT</td>
<td>INZ, SHIFT</td>
</tr>
<tr>
<td>HALT</td>
<td>00H</td>
</tr>
</tbody>
</table>

Q08. A memory system has a total of 8 memory chips, each with 12 addresses lines and 4 data lines. The total size of the memory system is
- (a) 4 Kbytes
- (b) 32 Kbytes
- (c) 48 Kbytes
- (d) 64 Kbytes

Q10. The following program is written for an 8085 microprocessor. To add two bytes located at memory addresses 1000H and 10FFH

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADD L</td>
<td>1000H</td>
</tr>
<tr>
<td>ADD H</td>
<td>10FFH</td>
</tr>
<tr>
<td>ADD M</td>
<td>MOV M</td>
</tr>
</tbody>
</table>
GATE-2001 (EE) - 2 marks
Q12. An 8085 microprocessor is executing the program given below:

MOV A, 10H
MOV B, 10H
BACK: NOP
ACD B
RLC
HLT

The number of lines that the operation NOP will be executed is equal to:
(a) 1 (b) 2 (c) 3 (d) 4

GATE-2000 (EE) - 1 mark
Q13. Which one of the following is not a vectorised interrupt?
(a) TRAP (b) INTR (c) RST 7.5 (d) RST 3

GATE-1999 & 1996 (EE)

GATE-1997 (EE)

Q14. In a microprocessor, the address of the next instruction to be executed is stored in:
(a) stack pointer (b) address latch (c) program counter (d) general purpose register

Q15. The range of addresses for which the memory chip shown in figure will be selected is from _______ to _______. - 2 marks

GATE-1996 (EE)

Q16. In an 8085 microprocessor, the following instructions may result in change of accumulator contents and change in status flags. Choose the correct answer for each instruction:
(a) ANL A, 0Fh; A = No change; Cy = 1; Ac = No change;
(b) XRA A; (Q) A = No change; Cy = 1; Ac = 1;
(c) CMP r7; (Q) A = No change; Cy = 1; Ac = 0;
(d) A = No change; Cy = 1; Ac = 0

GATE-1995 (EE)

GATE-1994 (EE) - 1 mark
Q17. In an 8085 microprocessor, after the execution of XRA A instruction:
(a) (e) carry flag is set
(b) the accumulator contains FFH
(c) the zero flag is set
(d) the accumulator contents are shifted left by one bit

GATE-1993 (EE) - 1 mark
Q18. The context of the accumulator in an 8085 microprocessor is altered after the execution of the instruction:
(a) CMP C (b) CR 3A (c) ANL 5C (d) ORA A

GATE-1991 (EE)

GATE-2009 (EE)

Q19. Three devices A, B & C have to be connected to a 8085 microprocessor. Device A has highest priority and device C has the lowest priority. In which of the following is correct assignment of interrupt inputs?
(a) with TRAP, B uses RST 5.5 and C uses RST 5.6
(b) uses RST 5.6
(c) uses RST 5.6 and C uses RST 7.5
(d) A uses RST 5.5, B uses RST 6.5 and C uses RST 7.5

GATE-2009 (EE)

Q20. Consider a system consisting of a microprocessor, memory, and peripheral devices connected by a common bus. During DMA data transfer, the microprocessor:
(a) only reads from the bus
(b) only writes to the bus
(c) both reads from and writes to the bus
(d) neither reads from nor writes to the bus

Notes:

GATE-2001 (EE)

GATE-2000 (EE)

GATE-1999 & 1996 (EE)

GATE-1997 (EE)

GATE-1996 (EE)

GATE-1995 (EE)

GATE-1994 (EE)

GATE-1993 (EE)

GATE-2009 (EE)

GATE-2001 (EE)

GATE-1997 (EE)

GATE-1996 (EE)

GATE-1995 (EE)

GATE-1994 (EE)

GATE-1993 (EE)

GATE-2009 (EE)

Notes:
Q22. A 2K x 8-bit RAM is interfaced to an 8085 microprocessor. If the address of the first memory location in the RAM is 3500 H, the address of the last memory location will be — mark
(a) 1FFF H
(b) 4FFF H
(c) 3FFF H
(d) 7FFF H

GATE: 2009 (E)

Q23. A part of the program written for an 8085 microprocessor is shown below. When the program execution reaches LOOP, the value of register C will be — marks
SUB A
MOV C,A
INC A
JC LOOP

LOOP2: NOP

(a) 03 H
(b) 64 H
(c) 09 H
(d) 100 H

GATE: 2007 (E)

Q24. A snapshot of the address, data, and control buses of an 8085 microprocessor executing a program given below is — marks

Address
2050 H
2051 H
2052 H
2053 H

Data
01H
24H
3FH
D1H

Control
LDFM: Logic High
HLA: Logic High
WM: Logic Low

The assembly language instruction being executed is
(a) IN 24 H
(b) INH 23 H
(c) OUT 24 H
(d) OUT 79 H

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GATE: 2007 (E)

Q25. A six-bit signed integer in 8th complement form is read into the accumulator of an 8085 microprocessor from an I/O port using the following assembly language program segment and symbolic addresses.
BEGIN: JR POINT
INC BEGIN
RAE
END: HLT

This program
(a) handles tens reading a negative number
(b) handles thousands reading a positive number
(c) handles thousands reading a zero
(d) never fails — marks

GATE: 2004 (E)

Q26. A memory mapped I/O device has an address of 0FFH, which of the following 8085 instructions outputs the content of the accumulator to the I/O device? — marks
(a) LDX #H, 0FFH
(b) LDX H, 0FFH
(c) MOV M, A
(d) OUT M
(e) LDI H, 0FFH
(f) LDI H, 0FFH

GATE: 2004 (E)

Q27. An 8085 assembly language program is given as follows. The execution time of each instruction is given against the instruction in terms of T-states. — marks

Instruction
T-state
IBH B, 00 H
7 T
LOOP: MOV C, 00 H
27 T
DCR C
27 T
OUT 40 H
4 T
MVI 40 H
7 T

The execution time of the program in terms of T-states is
(a) 247 T
(b) 250 T
(c) 244 T
(d) 257 T

GATE: 2004 (E)

Q28. The time period of a square wave in the audio frequency range is measured using an 8085 microprocessor by feeding the square wave to one of the four inputs, namely, RST 7.5, INT 0, RST 5.5 or INT 1. The algorithm used starts a timer at the beginning of a time period, stops the timer at the beginning of the next time period and reads the timer values for time measurement. Which of the following instructions should be followed for this application?
(a) INTR
(b) RST 5.5
(c) RST 7.5
(d) RST 6.5

GATE: 2004 (E)

Q29. An 8-bit microcontroller has an external interrupt in the memory map from address 00H to 07FH. The memory of bytes from this address can store
(a) 8192 (b) 8096 (c) 8192 (d) 8000

GATE: 2004 (E)

Q30. In an 8085 microprocessor, which one of the following is the correct sequence of the machine cycles for the execution of the DCR M instruction? — mark
(a) op-code fetch
(b) op-code fetch, memory read, memory write
(c) op-code fetch, memory read
(d) op-code fetch, memory write, memory write

GATE: 2004 (E)
Q31. A microprocessor has an instruction XOR (r1, r2), which performs an exclusive OR operation of registers r1, r2 and stores the result in r1. After the following instructions are executed what will be the following result?

(xor) (r, r1)
XOR (r, r2)
XOR (r1, r2)

(a) the contents of r1 is half sum of r1 and r2
(b) the contents of r2 is half sum of r1 and r2
(c) the contents of r1 and r2 remain unaltered
(d) the contents of r1 and r2 are swapped — 1 mark

Q32. In an 8085 microprocessor, the value of Slack Pointer (SP) is 2010H and top of UR stack is 1234H before the following code is executed. The value of the UR register pair after the following code is executed is — 2 marks

LW H, 0000H
PUSH H
PUSH H
POP B
DAF SP
XCHG
GATE 1904 (ED)

(a) 200E H (b) 200C H (c) 2010 H (d) 1234 H

Q33. The vector address corresponding to the software interrupt RT 7 in 8085 microprocessor is — 1 mark

(a) 0017 H (b) 0027 H (c) 0037 H (d) 0700 H

Q34. The following 8085 instructions are executed sequentially:

XRA A
MOV L, A
MOV H, L
INH H
DAF H

After execution, the content of HL register pair is — 2 marks

(a) 0000 H (b) 0101 H (c) 0010 H (d) 0002 H

Q35. Some of the pins of an 8085 CPU and their functions are listed below. Identify the correct answer that matches the pins to their respective functions — 1 mark

 tossed: 75-1, Selects I/O or memory.
 — 1 mark

G: 80/00, G: Data, D: Data address and data bus
R: 0, O: Any unaddressed interrupt
S: ALE, S: B l a s k DMA operation
D: B: Clock
S: Selects BCD mode operation

(a) P-0, Q-2, R-1, S-4 (b) P-4, Q-1, R-5, S-3
(c) P-3, Q-4, R-1, S-2 H P-2, Q-3, R-6, S-1

Q36. A ROM is interfaced to an 8085 CPU as indicated in figure. The address range occupied by the ROM is — 2 marks

(a) 0000H – 0FFF H (b) 0000H – 1FFF H
(c) 0000H – 0010H (d) 0000H – 000FH

Q37. In an 8085 system containing 8K x 8 ROM any word of RAM, the ROM is selected when A15 is 0 and ROM is selected when A15 is 1. A13 and A14 are ignored. The CPU executes the following program — 2 marks

MOV A, 00 H
STA 0000 H
DEC A
STA 0002 H
RET

The content of memory location 0000 H after the execution of the RET instruction is — 2 marks

(a) FF H (b) FF H (c) 01 H (d) 00 H

GATE 206-ED/ED

Q38. In an Intel 8085 microprocessor the address bus and data bus are — 1 mark

(a) Non-multiplexed (b) Multiplexed
(c) Duplicated (d) Same as control bus

Q39. In an 8085-based system the subroutine TEST is given below and called by another program. When the processor returns from the subroutine TEST, the value in the accumulator will be — 1 mark

TEST: MOV A, 00 H CALL TEST
TEST: INR A
TEST: RET

(a) 01 H (b) 05 H (c) 20 H (d) FF H

Q40. A simple microcomputer system is constructed using Intel 8085 microprocessor, an 8156 RAM and an 8355 I/O chip. The chip enable (CE) of 8156 and chip enable (CE) of 8355 are connected to the address line A12 of 8085. The address of port A of the 8156 chip is — 2 marks

(a) 21 H (b) 12 H (c) 11 H (d) 20 H

Table: 8085

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Table: 8085

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Q41. The 14-bit timer of 8058 is loaded with the counter value of
0705 H. The timer input is connected to a clock with a
frequency of 800 KHz. The timer is programmed to
produce a continuous square wave output. The
frequency of the square wave output is — 2 marks
(a) 400 KHz
(b) 800 KHz
(c) 400 Hz
(d) 2000 KHz

GATE-1991 (E3)

Q42. In a microprocessor with 16 address and 12 data lines, the
maximum number of opcodes is — 1 mark
(a) 2^16  (b) 2^24  (c) 2^32  (d) 2^9

Q43. An n-bit microprocessor has n-bit
(a) flag register  (b) instructions register
(c) data registers  (d) program counter

Q44. In 8085 microprocessor, CY flag may be set by the
instruction
(a) SUB  (b) INX  (c) CMA  (d) ANA

Q45. Microprocessor 8085 regulates control of the bus — 1 mark
(a) immediately after HLDA goes low
(b) immediately after HLDA goes high
(c) after half clock cycle after HLDA goes low
(d) after half clock cycle after HLDA goes high

GATE-2000 (E1)

Q46. Find the correct match among the following in the
content of an 8085 microprocessor — 1 mark
P: DMA  1. Program counter transfer instruction
Q: LXI  2. Data movement instruction
R: RST  3. Interrupt instruction
S: JMP  4. Arithmetic instruction
(a) P=4, Q=2, R=3, S=1
(b) P=2, Q=3, R=4, S=6
(c) P=1, Q=2, R=3, S=4
(d) P=4, Q=3, R=2, S=1

Q47. In an 8085 microprocessor, the Stack Pointer (SP) and
Program Counter (PC) register contain the number the
number F000 and 2400 in hex respectively. The contents
of the registers after execution of the instruction CALL
E000 would be — 1 mark
(a) PC : F003  SP : 2400
(b) PC : E000  SP : 2400
(c) PC : E000  SP : FF0E
(d) PC : E000  SP : 23FE

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Q48. 2K bytes of ROM have to be interfaced to an 8085
microprocessor using one EEPROM chip. The relevant
pins of the EEPROM are shown in fig. The address space
assigned to the ROM chip in hex is C000 CFFF H — 5 Marks
(a) Show how the address and data lines of the 8085
are to be connected to those of the EEPROM.
(b) Design the address decoding circuit whose output is
to be connected to the chip enable pin of the
EEPROM chip using only 2-input AND gate and
inverters.

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Q35. In the circuit shown, the device connected to VS can have address in the range of

(a) 2000 – 21FF  (b) 2000 – 22FF  (c) 2000 – 23FF  (d) F000 – F3FF

GATE-2010 (EEE)

Q36. When a "CALL Adder" instruction is executed, the CPU cenous the following sequential steps-(a) Internally:
Note: (R) means content of register R. — 1 Marks
(i) R1 means content of memory location pointed to by R1.
(ii) PC means Program Counter
(iii) SP means Stack Pointer.

(a) (SP) + 1 = SP
(b) (SP) + 1 = Address
(c) (SP) + 1 = (PC)
(d) (SP) + 1 = (SP)

Q37. The subroutine SB65 glass below is executed by an 8085 processor. The value in the accumulator immediately after execution of the subroutine will be: — 1 Marks

```
;  MOV A, 13H
;  MOV C, A
;  ADD A
;  SUB A
;  MOV A, 14H
;  SUB A
;  ADD A
;  MOV A, 15H
;  SUB A
;  ADD A
```

(a) 11H  (b) 13H  (c) 5FH  (d) AAH

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Q37. In an 8085 processor, the main program calls the subroutine SUB 1 given below. When the program was to the main program after executing SUB 1, the value in the accumulator is — 2 Marks

<table>
<thead>
<tr>
<th>Address</th>
<th>Opcode</th>
<th>Mnemonic</th>
</tr>
</thead>
<tbody>
<tr>
<td>2000</td>
<td>3E 00</td>
<td>SUB1</td>
</tr>
<tr>
<td>2001</td>
<td>6H 00</td>
<td>MV A, 60H</td>
</tr>
<tr>
<td>2002</td>
<td>00 00</td>
<td>CALL SUB2</td>
</tr>
<tr>
<td>2003</td>
<td>3C 32</td>
<td>SUB2 INR A</td>
</tr>
<tr>
<td>2004</td>
<td>C9 2F</td>
<td>RET</td>
</tr>
</tbody>
</table>

(a) 00 H  (b) 01 H  (c) 12 H  (d) 03 H

Q38. An 8-bit DAC is interfaced with a microprocessor having 16 address lines (A0, …, A15) as shown in the figure. A possible valid address for this DAC is

(a) 3000 H  (b) 4000 H  (c) 0FF00 H  (d) C000 H

**KEY**

- 01.d: 03 03 04 00 04 06 02 07 08
- 09 10 11 12 13 14 15 16
- 17 18 19 20 21 22 23 24
- 25 26 27 28 29 30 31 32
- 33 34 35 36 37 38 39 40
- 41 42 43 44 45 46 47 48
- 49 50 51 52 53 54 55
- 56 57 58 59 00 01

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135

Additional Questions

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10. Which of the following ADCs use sampling in its operation?
   (a) Sigma-delta ADC
   (b) Counterc ramp converter
   (c) Successive Approximation Register ADC
   (d) Flash Converter

11. In the circuit shown in the above figure, the value of output $V_4$ is
   (a) $+6\,\text{V}$
   (b) $-9\,\text{V}$
   (c) $-6\,\text{V}$
   (d) $+9\,\text{V}$

12. In the logic equation $A(A + B + C) + B(C + A + B + C) + A = 1$, if $C = \overline{A}$, then
   (a) $A + B = 1$
   (b) $A + B = 1$
   (c) $A + B = 1$
   (d) $A = 1$

13. A gate having two inputs $(A, B)$ and one output $(Y)$ is implemented using a 4-to-1 multiplexer as shown in Fig. A. $(A_1, A_0)$ are the control bits and $b_1, b_2$ are the inputs to the multiplexer. The gate is
   (a) NAND
   (b) NOR
   (c) XOR
   (d) OR

14. In Fig. U1 is a 4-bit binary synchronous counter with synchronous clear. $Q_1$ is the LSB and $Q_4$ is the MSB of the output.

   The circuit shown in Fig. represents a
   (a) mod 2 counter
   (b) mod 3 counter
   (c) mod 4 counter
   (d) mod 5 counter

---

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15. An increase in the value of the hold capacitor in a simple hold-and-man circuit results in
(a) decrease in the acquisition time and increase in the drop-out rate
(b) decrease in the acquisition time and decrease in the drop-out rate
(c) increase in the acquisition time and increase in the drop-out rate
(d) increase in the acquisition time and decrease in the drop-out rate

16. A 4-bit serial-in-parallel-out shift register is used with a feedback as shown in Fig. The shifting sequence is Q_4 → Q_0 → Q_3 → Q_1.

If the output is 0100 initially, the output repeter after
(a) 4 clock cycles  (b) 6 clock cycles  (c) 15 clock cycles  (d) 16 clock cycles

17. Fig. shows a section of a Programmable Logic Device (PLD).

The Boolean expression implemented in the PLD is
(a) A + BC + AB
(b) A + B + ABC
(c) A + B + ABC
(d) A + B + ABC

18. For an 8-bit digital-to-analog converter having reference voltage of 3 V, the least significant 4 bits of the input are grounded and the most significant 4 bits are driven by 4-bit data from a binary counter. The maximum obtainable peak-to-peak amplitude of a waveform at the output of the digital-to-analog converter is
(a) 4 V  (b) 6 V  (c) 7.2 V  (d) 7.5 V

19. Which one of the following Boolean expressions is NOT correct?
(a) x + y = x y
(b) x + y = x y
(c) x + y = x y
(d) x + y = x y

20. A Boolean function can be expressed
(a) as sum of minterms or product of minterms
(b) as product of maxterms or sum of minterms
(c) as product of maxterms and sum of minterms
(d) as product of sum of minterms and sum of product of minterms

21. Among the following logic families, the one having the lowest power dissipation and highest noise margin is
(a) Schottky TTL  (b) TTL  (c) ECL  (d) CMOS

22. The characteristic equation of a level triggered T flip-flop, with T as input and Q* as output is
(a) Q_{n+1} = T \cdot Q + \overline{T} \cdot Q*
(b) Q_{n+1} = T
(c) Q_{n+1} = \overline{Q}
(d) Q_{n+1} = T \cdot Q + \overline{T} \cdot \overline{Q}

23. A Combinational circuit accepts 2-bit binary number and outputs its square in binary. To design this circuit using a ROM, the minimum size of ROM required is
(a) 2 x 2  (b) 4 x 2  (c) 4 x 4  (d) 8 x 4

24. For the truth table given in Fig., the minimized Boolean expression is
(a) p = x \cdot y \oplus z
(b) p = x \cdot y \oplus z
(c) p = x \cdot y \oplus z

25. The Boolean function \( F(A, B, C) = \overline{F}(0, 2, 4, 7) \) is to be implemented using a 4 x 1 multiplexer shown in Fig. Which one of the following choices of inputs to multiplexer will realize the Boolean function?
(a) \( \{I_0, I_1, I_5, I_6, I_7\} = (0, A, C, B) \)
(b) \( \{I_0, I_1, I_5, I_6, I_7\} = (1, B, C, A, B) \)
(c) \( \{I_0, I_1, I_5, I_6, I_7\} = (0, 1, A, C, B) \)
(d) \( \{I_0, I_1, I_5, I_6, I_7\} = (0, 1, A, C, B) \)

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26. An edge triggered synchronous binary counter is provided with a clock (CLK) and control inputs: active low clear (CLR), active high load (L) and active high count (C). The correct matching combination between Column A and Column B is (JTO):

A. 1. (CLK, CLR, L, C) = (1, 1, 1, 1, X)  
   B. No change

2. (CLK, CLR, L, C) = (1, 0, 0, 1)  
   C. Load inputs

3. (CLK, CLR, L, C) = (X, 0, X, X)  
   D. Count next binary state

4. (CLK, CLR, L, C) = (X, 1, 0, 0)  
   E. Clear outputs

Where X = don’t care.

(a) 1-Q, 2-L, 3-N, 4-P  
(b) 1-P, 2-Q, 3-R, 4-S  
(c) 1-Q, 2-L, 3-P, 4-S  
(d) 1-P, 2-Q, 3-S, 4-R

27. A 5-bit serial adder is implemented using two 5-bit shift registers, a full adder and a D flip-flop. The two binary words to be added are 11011 and 11011. The sum of the two numbers is stored in one of the shift registers and the carry in the D flip-flop. Assuming that the D flip-flop is set initially, the content of the sum shift register and the D flip-flop respectively are (JTO):

(a) 10111 and 0  
(b) 11011 and 1  
(c) 11101 and 0  
(d) 10111 and 1

28. The Boolean expression \((A + B)(A + B)\) is equivalent to a two-input (EEE-JTO):

A. NAND gate  
B. NOR gate  
C. X-OR gate  
D. X-NOR gate

29. The minimum number of MOS transistors required to make a dynamic RAM cell is (EEE-JTO):

(a) 1  
(b) 2  
(c) 3  
(d) 4

30. How many minimum number of NOR gates are required to realize a two-input X-OR gate? (EEE-JTO):

(a) 2  
(b) 3  
(c) 4  
(d) 5

31. The sequential circuit shown in Fig. will act as (EEE-JTO):

(a) Mod – 1 counter  
(b) Mod – 2 counter  
(c) Mod – 1 counter  
(d) Mod – 4 counter

---

32. The total number of Boolean functions that can be constructed for \(n\) Boolean variables is (DRDO-CSE):

(a) \(2^n\)  
(b) \(2^{2^n}\)  
(c) \(2^n\)  
(d) \(2^n\)

33. Consider two 4-bit numbers \(A = A_3A_2A_1A_0\) and \(B = B_3B_2B_1B_0\) and the expression \(x_i = A_iB_i + A_iB_i\) for \(i = 0, 1, 2, 3\). The expression \(A_3B_3 + x_1A_2B_2 + x_2A_1B_1 + x_3A_0B_0\) evaluates to 1 if (DRDO-CSE):

(a) \(A = B\)  
(b) \(A \neq B\)  
(c) \(A > B\)  
(d) \(A < B\)

34. An odd function involving three Boolean variables is (DRDO-CSE):

(a) \(\sum (1, 3, 5, 7)\)  
(b) \(\sum (0, 2, 4, 6)\)  
(c) \(\sum (2, 4, 7)\)  
(d) \(\sum (0, 3, 5, 6)\)

35. How many 2-to-4 line decoders with enable input are needed to construct a 4-to-16-line decoder? (DRDO-CSE):

(a) 4  
(b) 5  
(c) 6  
(d) 8

36. The function \(f(A, B, C, D) = \sum (5, 7, 9, 10, 11, 13, 15)\) is independent of variable(s) (DRDO-CSE):

(a) \(B\)  
(b) \(C\)  
(c) \(A\) and \(C\)  
(d) \(D\)

37. \((3527)_{10}\) is equivalent to (DRDO-CSE):

(a) \((757)_{16}\)  
(b) \((1879)_{10}\)  
(c) \((131113)_{2}\)  
(d) All of these

38. How many flip-flops will be complemented in a 10-bit binary ripple counter to reach the next count after 1001101111? (DRDO-CSE):

(a) 3  
(b) 4  
(c) 6  
(d) 10

39. An 8 x 1 multiplexer has input \(A, B\) and \(C\) connected to the selection input \(s_0, s_1\) and \(s_2\) respectively. The data input to the \(s_3\) are as follows: \(L_0, L_1, L_2, L_3, L_4, L_5\) and \(L_6, L_7\). The Boolean functions that the multiplexer implements is (DRDO-CSE):

(a) \(f(A, B, C, D) = \sum (1, 6, 7, 9, 10, 11, 12)\)  
(b) \(f(A, B, C, D) = \sum (0, 5, 3, 11, 12)\)  
(c) \(f(A, B, C, D) = \sum (1, 3, 5, 7, 9, 11, 13, 15)\)  
(d) \(f(A, B, C, D) = \sum (0, 1, 4, 5, 6, 12)\)

40. The characteristic equation of a T flip-flop is given by (ISRO):

(a) \(Q(n+1) = TQ + TQ\)  
(b) \(Q(n+1) = \overline{T}\)  
(c) \(Q(n+1) = Q\)  
(d) \(Q(n+1) = TQ + \overline{TQ}\)

41. A clock state machine's output depends on (DRDO-CSE):

(a) State and outputs  
(b) Inputs  
(c) State  
(d) State and inputs
KEY
41. D

143. Additional Questions

PUBLIC SECTOR EXAMINATION QUESTIONS (MICROPROCESSOR) - 2009

01. A microcontroller differs from a microprocessor in terms of (CR)
(a) I/O interfaces and instruction decoding
(b) Memory configuration and I/O interfaces
(c) Data bus width and clock speed
(d) Memory configuration and instruction decoding

02. An 8-bit microcontroller has an external RAM with the memory map from 8000H to 9FFFH. The number of bytes this RAM contains is (CR)
(a) 8192
(b) 8193
(c) 8191
(d) 8000

03. Consider the following program for 8085

XRA A
LXI B, 1000H
LOOP: DCR B
INZ LOOP
The loop will be executed
(a) 8 times
(b) once
(c) 17 times
(d) infinite times

04. Which one of the following statements about the 8085 is TRUE? (CR)
(a) Only accumulator can be loaded with an 8-bit number in a single instruction.
(b) The processor can be interrupted even when it executesHLT instruction.
(c) When HOLD input is activated, the processor can execute register-to-register instructions.
(d) The program and data memories are separate.

05. The contents of the HL, register pair after the execution of the following program on the 8085 are (CR)

LXI B, 2095H
LXI H, 2095H
PUSH B
XTHL
POPB
HLT
(a) 2095H
(b) 2095H
(c) 2095H
(d) 8FDFH

06. When the 8085 receives an interrupt on its INTR pin, (CR)
(a) the program is directly transferred to a fixed call location
(b) 8055 waits till an interrupt acknowledgement is received and transfers program to a fixed call location
(c) the call location is determined by an external device
(d) the program is transferred to a call location indicated by MC register pair

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07. The figure shows an interfacing circuit for the 8085 microprocessor to read an 8-bit flag from an external device.

The appropriate instruction for reading the data is
(a) MVI A, FAH (b) IN F F AH (c) IN FF AH (d) LDA FF AH

86. In a 8085 microprocessor system, the active low chip select (CS) signal is generated by presetting address lines A15—>A0 through a inputs NAND gate. For selecting the address range CO0 to CF0F, the inputs to the NAND gate are

(a) A0, A1, A2, A3, A4, A5, A6, A7
(b) A0, A0, A0, A0, A0, A0, A0, A0
(c) A0, A1, A2, A3, A4, A5, A6, A7
(d) A0, A1, A2, A3, A4, A5, A6, A7

89. In the context of 8085 microprocessor, the correct switching combination between Column A and Column B is

<table>
<thead>
<tr>
<th>Column A</th>
<th>Column B</th>
</tr>
</thead>
<tbody>
<tr>
<td>P. ALE</td>
<td>1. Reset accumulator left</td>
</tr>
<tr>
<td>Q. PWL</td>
<td>2. Compare with accumulator</td>
</tr>
<tr>
<td>R. PWL</td>
<td>3. Program status word</td>
</tr>
<tr>
<td>S. RLC</td>
<td>4. Address latch enable</td>
</tr>
<tr>
<td>T. RLC</td>
<td>5. Program stack word</td>
</tr>
<tr>
<td>U. RLC</td>
<td>6. Arithmetic logic enabled</td>
</tr>
<tr>
<td>V. RLC</td>
<td>7. Complement accumulator</td>
</tr>
<tr>
<td>W. RLC</td>
<td>8. Reset accumulator left through carry</td>
</tr>
</tbody>
</table>

(a) P4, Q5, R2, S4 (b) P4, Q3, R2, S4 (c) P6, Q5, R2, S4 (d) P6, Q5, R7, S1

10. A 8085 microprocessor program uses all available Jump instructions, each only once. For this program, the total memory (in bytes) occupied by the Jump instructions is

(a) 30 (b) 27 (c) 24 (d) 18

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143. Additional Questions

ACE Academy

11. The contents of the memory location 2068 H after the execution of the following 8085 program is

LHBL 2074H
MTL A, 4FH
MVI C, 08H
INLB C
ANI 0FH
STAX B
HLT

(a) 04H (b) 07H (c) 69H (d) 0FH

12. An arithmetic operation in the 8085 microprocessor sets the sign and parity flags. The contents of the accumulator after the execution of the operation can be

(a) 1011 0100 (b) 0010 1101 (c) 1010 1101 (d) 0110 0111

13. An instruction in the 8085 microprocessor that requires both memory read and write machine cycle is

(a) MVI M, RF (b) LHD 808H (c) RST 1 (d) ADD M

14. The duration of one T-state in the 8085 microprocessor that uses a crystal of 5.00 MHz is

(a) 0.2 μs (b) 0.4 μs (c) 2.5 μs (d) 5.0 μs

15. The range of the address of the RAM which is interfaced to a microprocessor as shown in fig. 11 is

(a) 1400 - 17FF (b) E400 - E7FF (c) F000 - F7FF (d) 7400 - 7FFF

16. After the execution of the following program in the 8085 microprocessor, the contents of

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ACE Academy  Additional Questions  144
the accumulator are (ELECTRICAL, JITO)

<table>
<thead>
<tr>
<th>Address</th>
<th>Code</th>
<th>Microcontroller</th>
</tr>
</thead>
<tbody>
<tr>
<td>205A</td>
<td>3E 20</td>
<td>MPU 3, 20H</td>
</tr>
<tr>
<td>205C</td>
<td>2A, 3A 20</td>
<td>UHLD 203AH</td>
</tr>
<tr>
<td>205F</td>
<td>66</td>
<td>AMD 64</td>
</tr>
<tr>
<td>2040</td>
<td>76</td>
<td>H1I</td>
</tr>
</tbody>
</table>

(a) 20H  (b) 40H  (c) 5EH  (d) 7CH

17. The size of address bus of a microprocessor is 20 bits and the size of data bus is 8 bits. What is the maximum number of RAM chips of size 64K x 4 that can be connected to this microprocessor? (DRDO-CSE)
(a) 8  (b) 16  (c) 24  (d) 32

18. Static RAM (DRDO-CSE)
(a) is a volatile memory  (b) is a non-volatile memory  (c) needs refreshing to retain the value  (d) contains static information, i.e., cannot be modified

19. Pick up the correct pair in which the first element refers to the addressing modes with minimum operand fetching time and the second one refers to the addressing modes with maximum operand fetching time. (DRDO-CSE)
(a) Register direct and memory indirect.  (b) Register direct and indexed indirect.  (c) Immediate and indirect indirect.  (d) Immediate and indexed.

20. While an instruction is executed, the Program Counter (PC) should contain the address of (DRDO-CSE)
(a) the current instruction  (b) the next sequential instruction  (c) operand  (d) the previous instruction

21. A memory system of size 16 K bytes is required to be designed using memory chips which have 12 address lines and 4 data lines each. Then the number of such chips required to design the memory system is (ISRO)
(a) 2  (b) 4  (c) 8  (d) 16

22. Number of address lines required to address 8 K bytes of memory is (JTO)
(a) 13  (b) 14  (c) 15  (d) 16

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<th>GATE H.T NO</th>
<th>RANK</th>
</tr>
</thead>
<tbody>
<tr>
<td>01</td>
<td>HARINARAYANAN K K</td>
<td>EC-7158116</td>
<td>7</td>
</tr>
<tr>
<td>02</td>
<td>SHAIR AZEEMUDDIN</td>
<td>EC-1430552</td>
<td>6</td>
</tr>
<tr>
<td>03</td>
<td>SREEKAR S</td>
<td>EC-7005081</td>
<td>9</td>
</tr>
</tbody>
</table>

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<thead>
<tr>
<th>S.NO</th>
<th>STUDENT NAME</th>
<th>GATE H.T NO</th>
<th>RANK</th>
</tr>
</thead>
<tbody>
<tr>
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<td>MALLADI HARIKRISHNA</td>
<td>CS-1396148</td>
<td>1</td>
</tr>
<tr>
<td>02</td>
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<td>CS-6109316</td>
<td>8</td>
</tr>
</tbody>
</table>

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<th>STUDENT NAME</th>
<th>GATE H.T NO</th>
<th>RANK</th>
</tr>
</thead>
<tbody>
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<td>GAURAV HAIR</td>
<td>ME-1530117</td>
<td>4</td>
</tr>
<tr>
<td>02</td>
<td>MITHIL P</td>
<td>ME-1566133</td>
<td>5</td>
</tr>
</tbody>
</table>

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<table>
<thead>
<tr>
<th>S.NO</th>
<th>STUDENT NAME</th>
<th>GATE H.T NO</th>
<th>RANK</th>
</tr>
</thead>
<tbody>
<tr>
<td>01</td>
<td>C VEERAIAH</td>
<td>EE-1910022</td>
<td>5</td>
</tr>
<tr>
<td>02</td>
<td>THEJOBSWARY NAIDU D</td>
<td>EE-1492267</td>
<td>7</td>
</tr>
</tbody>
</table>

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<tr>
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<th>STUDENT NAME</th>
<th>GATE H.T NO</th>
<th>RANK</th>
</tr>
</thead>
<tbody>
<tr>
<td>01</td>
<td>KAMANI DEEPESH HASIMUKHAL</td>
<td>IN-1290044</td>
<td>6</td>
</tr>
<tr>
<td>02</td>
<td>KARTHIKEYAN S</td>
<td>IN-1290364</td>
<td>8</td>
</tr>
</tbody>
</table>

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<table>
<thead>
<tr>
<th>S.NO</th>
<th>STUDENT NAME</th>
<th>GATE H.T NO</th>
<th>RANK</th>
</tr>
</thead>
<tbody>
<tr>
<td>01</td>
<td>ACPARTA PRIRANA U</td>
<td>CE-1270625</td>
<td>9</td>
</tr>
</tbody>
</table>

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